

59.(New) A memory apparatus according to Claim 55, wherein said inner battery is a rechargeable battery; and where said memory apparatus further comprising a recharge circuit to use said higher operating voltage from said digital source to rapid recharge said rechargeable battery during data transfer from said digital source to said memory apparatus.

60 (New) A memory apparatus according to Claim 55, wherein said memory apparatus is a personal audio player for playing vended audio programs, and wherein said digital source is an audio program vending machine.

### REMARKS

This Amendment is responsive to the paper identified above, and is responsive in any manner indicated below.

### PENDING CLAIMS

Claims 46-54 were pending in the application at the time of the Office Action, under consideration and subject to examination. Unrelated to any prior art rejection, appropriate claims have been added in order to refocus Applicant's claimed invention to features of present commercial interest. For example, new Claims 55-60 are submitted herein to adjust a clarify of Applicant's claimed invention, and find antecedent basis throughout the application, e.g., in Figure 10; at page 35, line 13 through page 35, line 15; and at page 36, line 19 through page 37, line 25. The

amendments to the claims are unrelated to any prior art or scope adjustment, and are simply refocused claims in which Applicant is presently interested. At entry of this paper, Claims 46-60 are pending for further consideration and examination in the application.

### **FOREIGN PRIORITY - PERFECTED**

As set forth in the Preliminary Amendment filed with the application on 22 June 2001, Applicant claims priority under 35 U.S.C. §119 of four JP applications, and the certified copies of the priority documents with certified English-language translations therefor were filed and acknowledged in prior application Serial No. 07/727,420.

It is courteously pointed out that there is no longer a requirement for certified translations of the priority documents, the requirement having been set forth in the 4 April 2002 Office Action. However, Applicant respectfully submits that, in accordance with 37 CFR §1.55 and MPEP §201, all of the certified copies and certified English-language translations of the priority documents already have been filed in a prior application upon which benefit is claimed in the present case under §120, and therefore, all of the requirements for perfection of the claim for foreign priority in this application have been completed. However, for the convenience of the Office, attached hereto are copies of the certified English-language translations as filed in the prior application.

Applicant now respectfully requires written acknowledgment of the perfection of foreign priority in the present application.

**REQUEST FOR TRANSLATIONS - TO BE FILED**

At Item 4 on pages 2 and 3 of the Detailed Action of 4 April 2002, it is suggested that it may benefit examination of the present application to have English-language translations of the foreign Patent Office Actions filed with the Information Disclosure Statement on 28 January 2002. Such translations are being prepared, and will be submitted to the Office upon completion.

**OBJECTIONS TO DRAWING CHANGES - TRAVERSED AS IMPROPER**

Filed concurrently with the Preliminary Amendment submitted with the present application was a Letter to the Official Draftsperson with proposed corrections, all of which had been previously approved and entered in the prior applications upon which benefit is claimed in the present case. Concurrently submitted with the proposed figure corrections were forty-six sheets of formal drawings for Figures 1-69 with the proposed drawing corrections completed thereon. In accordance with 37 CFR §1.121 and MPEP §608.02, the objection to the proposed figure corrections is improper because 37 CFR §1.84 relates to formal drawings, not proposed drawing changes. If there are objections to any of the forty-six sheets of formal drawings filed with the application, Applicant respectfully requires the Office to issue a Notice of Patent Draftsperson's Drawing Review Form PTO-948, to enumerate such objections. In the absence of an objection to or rejection of the forty-six sheets of formal drawings, Applicant respectfully requires written acknowledgment of the approval and entry of same.

In either event, Applicant courteously requests withdrawal of the improper objection to the drawings.

**DOUBLE PATENTING REJECTION - IMPROPER/NOT SUPPORTED**

At Items 7-15 on pages 4-7 of the Detailed Action, Claims 46-54 are rejected under the judicially-created doctrine of double patenting based on various claims published in USP 6,282,611 and Publication No. 2001/0037431.

The rejection based on the publication is respectfully traversed as improper, because the publication is the published version of the present application. There is absolutely no potential for double patenting under U.S. patent laws because the published version of the same application cannot be held against itself.

Further, the non-statutory double patenting rejection based on USP 6,282,611 is respectfully traversed because such rejection does not provide the factual analysis required for such rejections under U.S. patent law, i.e., the Examiner has not satisfied his/her initial burden to adequately support the rejection. More particularly, MPEP §804 providing guidance for examining states that:

Since the analysis employed in an obviousness-type double patenting determination parallels the guidelines for a 35 USC 103(a) rejection, the factual inquiries set forth in *Graham v. John Deere Co.*, 383 US 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 USC 103 are employed when making an obviousness-type double patenting analysis. These factual inquiries are summarized as follows:

(A) Determine the scope and content of a patent claim and the prior art relative to a claim in the application at issue;

(B) Determine the differences between the scope and content of the patent claim and the prior art as determined in (A) and the claim in the application at issue;

(C) Determine the level of ordinary skill in the pertinent art; and

(D) Evaluate any objective indicia of non-obviousness.

. . .



Any obviousness-type double patenting rejection should make clear:

(A) The differences between the invention defined by the conflicting claims - a claim in the patent compared to a claim in the application; and

(B) The reasons why a person of ordinary skill in the art would conclude that the invention defined in the claim in issue is an obvious variation of the invention defined in a claim in the patent.

The rejection does not make clear the differences, or the reasons why any person of ordinary skill in the art would conclude that the invention defined in the claim in issue is an obvious variation of the invention defined in a claim in the patent.

Accordingly, Applicant respectfully submits that the above analysis should be provided in order for the Examiner to satisfy his/her initial burden to support the rejection, or the rejection should be withdrawn.

In any event, Applicant respectfully requires withdrawal of any double patenting rejection based on the claims of its publication 2001/0037431. It is respectfully noted that such double patenting rejections may further have been obviated by the present refocusing of Applicant's claims.

#### **REJECTIONS UNDER 35 USC §103 - TRAVERSED**

All 35 USC §103 rejections (*i.e.*, the rejection of Claims 46 and 48-54 as being unpatentable over Kramer *et al.* (U.S. Patent 4,667,088) in view of Nomura *et al.* (U.S. Patent 4,779,138), and further in view of Jinguji (U.S. Patent 4,847,840) and Kramer (U.S. Patent 4,991,218); the rejection of Claim 47 as being unpatentable over Kramer *et al.* in view of Nomura *et al.*, Jinguji and Kramer, and further in view of Ukegawa (U.S. Patent 4,926,463); and the rejection of Claims 51-54 as being

unpatentable over Kramer *et al.* in view of Nomura *et al.*, and further in view of Jinguji, Kramer and Tarlow *et al.* (U.S. Patent 5,045,327)) are respectfully traversed based upon the following.

All descriptions of Applicant's disclosed and claimed invention, and all descriptions and rebuttal arguments regarding the applied prior art, as previously submitted by Applicant in any form, are repeated and incorporated herein by reference. Further, all Office Action statements regarding the prior art rejections are respectfully traversed. As additional arguments, Applicant respectfully submits the following.

In order to properly support a §103 obviousness-type rejection, both the teaching and the motivation to combine features must be present in the applied art. The applied art does not adequately support a §103 rejection because, at minimum, such applied art does not suggest the claimed limitations of Applicant's invention.

At the outset, reference is made to the decision of In re Fine, 5 USPQ 2d 1596 (Fed. Cir. 1988), wherein the Court pointed out that the PTO has the burden under §103 to establish a *prima facie* case of obviousness and can satisfy this burden only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references. As noted by the Court, whether a particular combination might be "obvious to try" is not a legitimate test of patentability and obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion supporting the combination. As further noted by the Court, one cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the

claimed invention. Applicant respectfully submits that the Examiner has picked and chosen features of the many references it was found necessary to apply to reject the claims, in a construct of Applicant's invention with hindsight knowledge of Applicant's own teaching, but such hindsight construction is forbidden.

In addition to the foregoing, the following additional remarks from Applicant's foreign representative are also submitted in support of traversal of the rejection and patentability of Applicant's claims.

The present invention is directed to a memory apparatus as a player comprising a playback function to store digital data and reproduce the stored data, a memory circuit, an inner battery (secondary battery) and a battery switch for switching a power supply for use in the apparatus. When the memory circuit stores digital data from a digital source as an external terminal connected thereto, the battery switch operates to switch power supply from the inner battery to a power supply of the digital source having a higher operating voltage than that of the inner battery. When the memory apparatus is operated in a state electrically isolated from the digital source, the battery switch operates to actuate the inner battery as a power supply for reproduction of the stored digital audio signal in the apparatus.

With this configuration, data transfer from the terminal to the memory apparatus can be made rapidly and simultaneously, and the lifetime of the secondary battery can be elongated. Refer to the present specification at page 35, line 13 to page 36, line 15, and page 21, line 21 to page 22, line 8, as well as Fig. 12.

A memory apparatus for a player according to the present invention includes a power supply having a lower operating voltage than that of a server (terminal) side, and a battery switch to automatically switch a supply source of the player to the

a battery switch to automatically switch a supply source of the player to the server-side power supply under connection between the server and the player for data transfer.

Such apparatus would not be obvious from the cited patents, either singly or in combination.

For example, the Office Action asserts at page 12, lines 15-22 thereof, that Tarlow teaches a battery in a playback module 20 and a power source in a digital record center 10. However, this patent does not disclose any specific structure or the like as to which power source in the module and the center is used when and how the power sources are used.

As well, none of the other applied references teach or suggest power supply switching as specified in the claims of this application, alone or in any combination.

As a result of all of the foregoing, it is respectfully submitted that the applied art (taken alone and in the Office Action combinations) would not support a §103 obviousness-type rejection of Applicant's claims. Accordingly, reconsideration and withdrawal of such §103 rejection, and express written allowance of all of the §103 rejected claims, are respectfully requested.

#### **EXAMINER INVITED TO TELEPHONE**

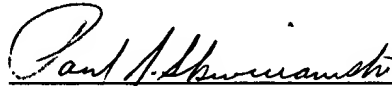
The Examiner is herein invited to telephone the undersigned attorney at the local D.C. area telephone 703-312-6600 to discuss any Examiner's Amendment or other suggested actions for accelerating prosecution and moving the present application to allowance.

**CONCLUSION**

This Amendment is being timely filed in the shortened statutory period for response set by the 2 April 2002 Action. Further, the claims added herein do not exceed the limit set for the total number of independent and dependent claims in an application. Therefore, no Petition or additional fee is believed required.

To whatever other extent is actually necessary, Applicant respectfully petitions the Commissioner for an extension of the due date for response to the Action mailed 4 April 2002. Please charge any deficiencies in appropriate fees to ATS&K Deposit Account No. 01-2135 (as Order No. 500.31310CX2).

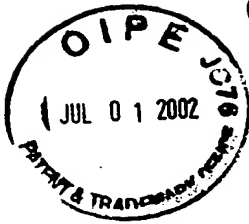
Respectfully submitted,



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**ATTACHMENTS:**

Copies of Certified English-Language  
Translations of JP 3-57930, JP 2-208072,  
JP 2-181402 and JP 3-57972



DECLARATION

**RECEIVED**

**JUL 03 2002**

**Technology Center 2100**

I, Michiyuki MORITA , a national of Japan, c/o Asamura Patent Office of 331-340, New Ohtemachi Building, 2-1, Ohtemachi-2-chome, Chiyoda-ku, Tokyo, Japan do hereby solemnly and sincerely declare:-

- 1) THAT I am well acquainted with the Japanese language and English language, and
- 2) THAT the attached is a full, true and faithful translation into the English language made by me of Japanese Patent Application No. 2-208072

The undersigned declares further that all statements made herein of his own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001, of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Signed this 31st day of January , 1994.

Michiyuki Morita

Michiyuki MORITA

2-208072

APPLICATION FOR PATENT

August 8, 1990

The Director-General  
The Patent Office

Title of the Invention: RECORDING AND REPRODUCTION  
SYSTEM

Number of Claim(s) for a Patent: 70

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List of the annexed documents:

- (1) Specification ----- 1 copy
- (2) Drawings ----- 1 copy
- (3) Power of Attorney ----- 1 copy
- (4) Duplicate of Application Form ----- 1 copy

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## SPECIFICATION

## 1 1. Title of the Invention

## RECORDING AND REPRODUCTION SYSTEM

## 2. Scope of Claim for a Patent

1. A recording and reproduction system comprising  
5 at least:

(1) a sound recording section including an A/D  
conversion section, a sound recording digital memory a  
sound recording control section, a sound recording  
display section and a sound recording operating section;  
10 and

(2) a reproduction section including a D/A  
conversion section, a reproduction semiconductor digital  
memory, a reproduction control section, a reproduction  
display section and a reproduction operating section;  
15 characterized in that the sound recording section and  
the reproduction section are separated from each other.

2. A recording and reproduction system as  
described in Claim 1, characterized in that the record-  
ing information desired by the user is selected from a  
20 large-capacity storage of the sound recording section in  
accordance with a content index and transferred to a  
small-capacity storage of the reproduction section.

3. A recording and reproduction system as  
described in Claim 2, characterized in that the sound

1 recording control section has at least one or more index  
address register, an address counter and a sound record-  
ing control circuit.

4. A recording and reproduction system as  
5 described in Claim 1, characterized in that the sound  
recording control section energizes the address counter  
on the basis of an index address designated by the sound  
recording operating section, and the input analog infor-  
mation is converted into digital information at the A/D  
10 conversion section and is held in the sound recording  
memory.

5. A recording and reproduction system as  
described in Claim 4, characterized in that the sound  
recording control section transfers an index address  
15 signal and digital information in order to transfer and  
write the digital information stored in the sound  
recording memory into the reproduction memory of the  
reproduction section.

6. A recording and reproduction system as  
20 described in Claim 1, characterized in that the sound  
recording control section transfers at least one or more  
signals indicating that the reproduction section is  
ready for writing to the sound recording section in  
order to transfer the digital information stored in the  
25 sound recording memory.

7 A recording and reproduction system as  
described in Claim 1, characterized in that the repro-  
duction control section includes at least an index

1 address register, a head address register, a voice  
presence/absence flag bit indicating the presence or  
absence of a voice file and an address counter.

8. A recording and reproduction system as  
5 described in Claim 1, characterized in that the repro-  
duction control section forms a pair of tables having at  
least an index address register, a head address register  
and a voice presence/absence flag bit indicating the  
presence or absence of a voice file, the reproduction  
10 control section being configured of at least one pair of  
table.

9. A recording and reproduction system as des-  
cribed in Claim 7, characterized in that the reproduc-  
tion control section is such that the last value of +1  
15 of the address counter for generating an address of the  
reproduction memory is fed back and set for each voice  
file to the head address register configured as a pair  
with the register for storing an index address.

10. A recording and reproduction system comprising  
20 at least:

(1) a sound recording section having a digital  
memory recorded with information, a sound recording  
control section, a sound recording display section and a  
sound recording operating section;

25 (2) a reproduction section having a D/A  
conversion section, a reproduction semiconductor digital  
memory, a reproduction control section, a reproduction  
display section and a reproduction operating section;

1 characterized in that the sound recording section and  
the reproduction section are separated from each other.

11. A recording and reproduction system comprising  
at least:

5 (1) a sound recording/reproduction section  
having an A/D conversion section, a sound recording/re-  
production digital memory, a D/A conversion section, a  
sound recording/reproduction control section, a sound  
recording/reproduction display section and a sound  
10 recording/reproduction operating section; and

(2) a reproduction section having a D/A  
conversion section, a reproduction semiconductor digital  
memory, a reproduction control section, a reproduction  
display section and a reproduction operating section;  
15 characterized in that the recording/reproduction section  
and the reproduction section are separated from each  
other.

12. A recording and reproduction system as  
described in Claim 1, characterized in that the repro-  
20 duction control section energizes the address counter on  
the basis of an index address designated by the repro-  
duction operating section, and the digital information  
stored and held in the reproduction memory is converted  
into analog information at the D/A conversion section  
25 and outputted out of the system.

13. A recording and reproduction system as  
described in Claim 3, characterized in that the index  
address register of the sound recording section is

1 configured of at least a memory of content read type  
capable of searching for the coincidence of the stored  
contents of the register.

14. A recording and reproduction system as  
5 described in Claim 7, characterized in that the index  
address register of the reproduction section and the  
head address register are configured of at least a  
memory of content read type capable of searching for the  
coincidence of the stored contents of the register.

10 15. A recording and reproduction system as  
described in Claim 9, characterized further by a  
mechanism for generating a head address of a voice file  
for converting the index address transferred with the  
voice file information sequentially as successive  
15 addresses of the reproduction memory in the case where  
the reproduction control section stores the digital  
information transferred from the sound recording section  
in the reproduction memory of the reproduction section.

16. A recording and reproduction system as  
20 described in Claim 15, characterized in that digital  
information is written in or read from the reproduction  
memory as a result of generation of a head address of  
the reproduction memory by said mechanism.

17. A recording and reproduction system as  
25 described in Claim 17, characterized in that the signal  
interface is connected at least mechanically, by radio  
or electromagnetic or electrostatic coupling, or in  
optical fashion.

- 1 18. A recording and reproduction system as  
described in Claim 1, characterized in that the sound  
recording memory is configured of at least a semi-  
conductor memory, an optical disk, a magnetic disk, a  
5 digital audio tape or the like large-capacity memory  
means.
19. A recording and reproduction system as  
described in Claim 1, characterized in that the capacity  
of the sound recording memory is equal to or larger than  
10 that of the reproduction memory.
20. A recording and reproduction system as  
described in Claim 1, characterized by being configured  
of a table in a pair having at least an index address  
register, a head address register and an audio file flag  
15 bit in order to store the digital information of the  
reproduction section in blocks into which the reproduc-  
tion memory is divided, the system having one or more  
pairs.
21. A recording and reproduction system as  
20 described in Claim 1 or 5, characterized in that in the  
case where the reproduction memory is made of a DRAM,  
the refreshing of the DRAM is demanded and controlled  
from the sound recording section at the time of transfer  
and writing from the sound recording section to the  
25 reproduction section.
22. A recording and reproduction system as  
described in Claim 21, characterized in that the  
refreshing of the DRAM is controlled by the reproduction

1 section before or after transfer and writing of the  
digital information.

23. A recording and reproduction system as  
described in Claim 21, characterized in that the re-  
5 freshening of the DRAM is controlled by the reproduction  
section before insertion of the reproduction section  
into the sound recording section or after pulling off of  
the reproduction section.

24. A recording and reproduction system as  
10 described in Claim 1, characterized in that the A/D  
conversion section, the sound recording memory and the  
sound recording control section of the sound recording  
section are disposed at least on the same semiconductor  
substrate.

15 25. A recording and reproduction system as  
described in Claim 1, characterized in that the D/A  
conversion section, the reproduction memory and the  
reproduction control section of the reproduction section  
are disposed at least on the same semiconductor  
20 substrate.

26. A recording and reproduction system as  
described in Claim 1, characterized in that the  
reproduction section includes a circuit for transmitting  
digital information and outputting a modulated electric  
25 wave outside, said modulated sound digital information  
being demodulated at a receiver and further outputted  
from earphone, speaker or the like as analog information  
through the A/D conversion section.

- 1 27. A recording and reproduction system as described in Claim 1, characterized in that the sound recording section includes at least a sound recording clock and a transfer/write clock, and the reproduction  
5 section includes at least a reproduction clock.
28. A recording and reproduction system as described in Claim 25, characterized in that the transfer/write clock is higher in speed than the sound recording clock or the reproduction clock.
- 10 29. A recording and reproduction system as described in Claim 16, characterized in that at least a buffer is inserted between the sound recording memory of the sound recording section and the reproduction memory of the reproduction section.
- 15 30. A recording and reproduction system as described in Claim 1, characterized in that a memory card, an IC card or the like is at least insertable into the reproduction section.
31. A recording and reproduction system as  
20 described in Claim 1, characterized in that the housing of the reproduction section is constructed of at least a flat surface having no adverse effect on insertion or having an uneven slot for insertion guide.
32. A recording and reproduction system as  
25 described in Claim 1, characterized in that the housing of the reproduction section has an insertion overlapping with the sound recording section, at least displaced



1 from the arrangement of the input operating section of  
the housing or the display section.

33. A recording and reproduction system as  
described in Claim 1, characterized in that the repro-  
5 duction semiconductor digital memory is configured of an  
EEPROM memory capable of writing electrically and  
erasing electrically, an EPROM memory capable of writing  
electrically and erasing by ultraviolet ray, a fuse ROM  
memory, a SRAM memory, a SRAM memory or DRAM memory  
10 backed up with a battery, or a combination of any of the  
memories.

34. A recording and reproduction system as  
described in Claim 10, characterized in that the digital  
memory recorded with information is constructed of at  
15 least a large-capacity storage device such as a  
semiconductor memory, an optical disk, a magnetic disk,  
a digital audio tape or the like including an EEPROM  
memory, an EPROM memory, a fuse ROME memory, a SRAM or  
DRAM memory backed up with a battery, or any  
20 combinations of the memories.

35. A recording and reproduction system as  
described in Claim 11, characterized in that the digital  
memory for reproducing the recorded sound is configured  
of at least a semiconductor memory, an optical disk, a  
25 magnetic disk, a digital audio tape or the like large-  
capacity storage device.

1 36. A method of sound recording and reproduction  
using a recording and reproduction system comprising at  
least:

(1) a sound recording section having an A/D  
5 conversion section, a sound recording digital memory, a  
sound recording control section, a sound recording  
display section and a sound recording control section;  
and

(2) a reproduction section having a D/A  
10 conversion section, a reproduction semiconductor digital  
memory, a reproduction control section, a reproduction  
display section and a reproduction operating section;  
characterized in that the sound recording section and  
the reproduction section are separated from each other.

15 37. A method of recording and reproduction using a  
recording and reproduction system as described in Claim  
1, characterized in that the recording information  
desired by the user is selected from the large-capacity  
storage of the sound recording section and transferred  
20 to the small-capacity storage of the reproduction  
section in accordance with a content index.

38. A method of sound recording and reproduction  
using a recording and reproduction system as described  
in Claim 2, characterized in that the sound recording  
25 control section has at least one or more index address  
registers, an address counter and a sound recording  
control circuit.

1 39. A method of sound recording and reproduction  
using a recording and reproduction system as described  
in Claim 1, characterized in that the sound recording  
control section energizes the address counter on the  
5 basis of an index address designated from the sound  
recording operating section, and the input analog infor-  
mation is converted into digital information by the A/D  
conversion section and held by being stored in the sound  
recording memory.

10 40. A method of sound recording and reproduction  
using a recording and reproduction system as described  
in Claim 4, characterized in that the sound recording  
control section transfers an index address signal and  
digital information in order to transfer and write the  
15 digital information stored in the sound recording memory  
into the reproduction memory of the reproduction  
section.

41. A method of sound recording and reproduction  
using a recording and reproduction system as described  
20 in Claim 1, characterized in that the sound recording  
control section transfers one or more signals indicating  
that the reproduction section is ready for writing, to  
the sound recording section, in order to transfer the  
digital information stored in the sound recording  
25 memory.

42. A method of sound recording and reproduction  
using a recording and reproduction system as described  
in Claim 1, characterized in that the reproduction

1 control section has at least an index address register,  
a head address register, a sound presence/absence flag  
bit indicating the presence or absence of an audio file  
and an address counter.

5 43. A method of sound recording and reproduction  
using a recording and reproduction system as described  
in Claim 1, characterized in that the reproduction  
control section has at least an index address register,  
a head address register and an audio presence/absence  
10 flag bit indicating the presence or absence of an audio  
file in the form of pairs, said table being configured  
of at least a pair.

44. A method of sound recording and reproduction  
using a recording and reproduction system as described  
15 in Claim 7, characterized in that the reproduction  
control section is such that the final value of +1 of  
the address counter for generating an address of the  
reproduction memory is fed back and set for each audio  
file to the head address register configured as a pair  
20 with the register for storing the index address.

45. A method of sound recording and reproduction  
using a recording and reproduction system, comprising at  
least:

(1) a sound recording section having a digital  
25 memory recorded with information, a sound recording  
control section, a sound recording display section and a  
sound recording operating section; and

1           (2) a reproduction section having a D/A  
conversion section, a reproduction semiconductor digital  
memory, a reproduction control section, a reproduction  
display section and a reproduction operating section;  
5 characterized in that the sound recording section and  
the reproduction section are separated from each other.

46.       A method of sound recording and reproduction  
using a recording and reproduction system, comprising at  
least:

10           (1) a sound recording/reproduction section  
having an A/D conversion section, a sound recording and  
reproduction digital memory, a D/A conversion section, a  
sound recording and reproduction control section, a  
sound recording and reproduction display section, and a  
15 sound recording and reproduction operating section;

          (2) a reproduction section having a D/A  
conversion section, a reproduction semiconductor digital  
memory, a reproduction control section, a reproduction  
display section and a reproduction operating section;  
20 characterized in that the sound recording section and  
the reproduction section are separated from each other.

47.       A method of sound recording and reproduction  
using a recording and reproduction system as described  
in Claim 1, characterized in that the reproduction  
25 control section energizes the address counter on the  
basis of an index address designated by the reproduction  
operating section, and the digital information held by  
being stored in the reproduction memory is converted

1 into analog information at the D/A conversion section  
and outputted out of the system.

48. A method of sound recording and reproduction  
using a recording and reproduction system as described  
5 in Claim 3, characterized in that the index address  
register of the sound recording section is configured of  
at least a memory of content read type capable of  
searching for the coincidence of the contents stored in  
the register.

10 49. A method of sound recording and reproduction  
using a recording and reproduction system as described  
in Claim 7, characterized in that the index address  
register and the head address register of the reproduc-  
tion section are configured of at least a memory of  
15 content read type capable of searching for the  
coincidence of the contents stored in the registers.

50. A method of sound recording and reproduction  
using a recording and reproduction system as described  
in Claim 9, characterized in that the reproduction  
20 control section includes a mechanism for generating a  
head address of the audio file for converting the index  
address transferred with the information of the audio  
file sequentially as successive addresses of the  
reproduction memory in the case where the digital  
25 information transferred from the sound recording section  
is stored in the reproduction memory of the reproduction  
section.

1 51. A method of sound recording and reproduction  
using a recording and reproduction system as described  
in Claim 15, characterized in that digital information  
is written into or read from the reproduction memory by  
5 the generation of the head address of the reproduction  
memory by the above-mentioned mechanism.

52. A method of sound recording and reproduction  
using a recording and reproduction system as described  
in Claim 1, characterized in that the signal interface  
10 between the sound recording section and the reproduction  
section is connected at least mechanically, by radio, or  
by electromagnetic or electrostatic coupling, or in  
optical fashion.

53. A method of sound recording and reproduction  
15 using a recording and reproduction system as described  
in Claim 1, characterized in that the sound recording  
digital memory is configured of at least a semiconductor  
memory, an optical disk, a magnetic disk, a digital  
audio tape or the like large-capacity storage device.

20 54. A method of sound recording and reproduction  
using a recording and reproduction system as described  
in Claim 1, characterized in that the capacity of the  
sound recording memory is equal to or larger than that  
of the reproduction memory.

25 55. A method of sound recording and reproduction  
using a recording and reproduction system as described  
in Claim 1, characterized by being constructed of a  
table in a pair having at least an index address

1 register, a head address register and an audio file flag  
bit in order to store the digital information of the  
reproduction section in blocks into which the reproduc-  
tion memory is divided, said table being configured of  
5 one or more pairs.

56. A method of sound recording and reproduction  
using a recording and reproduction system as described  
in Claim 1 or 5, characterized in that in the case where  
the reproduction memory is configured of a DRAM, the  
10 refreshing of the DRAM is demanded and controlled from  
the sound recording section at the time of transfer and  
writing from the sound recording to the reproduction  
section.

57. A method of sound recording and reproduction  
15 using a recording and reproduction system as described  
in Claim 21, characterized in that the refreshing of the  
DRAM is controlled by the reproduction section before or  
after transfer and writing of digital information.

58. A method of sound recording and reproduction  
20 using a recording and reproduction system as described  
in Claim 21, characterized in that the refreshing of the  
DRAM is controlled by the reproduction section before  
insertion of the reproduction section into the sound  
recording section or after pulling off of the reproduc-  
25 tion section.

59. A method of sound recording and reproduction  
using a recording and reproduction system as described  
in Claim 1, characterized in that the A/D conversion



1 section, the sound recording memory and the sound  
recording control section of the sound recording section  
are disposed at least on the same semiconductor  
substrate.

5 60. A method of sound recording and reproduction  
using a recording and reproduction system as described  
in Claim 1, characterized in that the A/D conversion  
section, the reproduction memory and the reproduction  
control section of the reproduction section are disposed  
10 at least on the same semiconductor substrate.

61. A method of sound recording and reproduction  
using a recording and reproduction system as described  
in Claim 1, characterized in that the reproduction  
section includes a digital information transmission  
15 circuit, an electric wave modulated is outputted  
outside, and the modulated audio digital information is  
demodulated at a receiver and further outputted from  
earphone, speaker or the like as analog information  
through the A/D conversion section.

20 62. A method of sound recording and reproduction  
using a recording and reproduction system as described  
in Claim 1, characterized in that the sound recording  
section has at least a sound recording clock and a  
transfer/write clock, and the reproduction section has  
25 at least a reproduction clock.

63. A method of sound recording and reproduction  
using a recording and reproduction system as described  
in Claim 25, characterized in that the transfer/write

1 clock is higher in speed than the sound recording clock  
or the reproduction clock.

64. A method of sound recording and reproduction  
using a recording and reproduction system as described  
5 in Claim 16, characterized in that a buffer memory is  
interposed at least between the sound recording memory  
of the sound recording section and the reproduction  
memory of the reproduction section.

65. A method of sound recording and reproduction  
10 section using a recording and reproduction system as  
described in Claim 1, characterized in that a memory  
card, an IC card or the like is at least insertable into  
the reproduction section.

66. A method of sound recording and reproduction  
15 using a recording and reproduction system as described  
in Claim 1, characterized in that the housing of the  
reproduction section has the means of insertion into the  
sound recording section configured of at least a flat  
surface having no adverse effect on the insertion or a  
20 flat surface with a rough slot for insertion guide.

67. A method of sound recording and reproduction  
using a recording and reproduction system as described  
in Claim 1, characterized in that the housing of the  
reproduction section has the overlapped portion for  
25 insertion thereof at least displaced from the  
arrangement of the input operating section or the  
display section of the housing.

1 68. A method of sound recording and reproduction  
using a recording and reproduction system as described  
in Claim 1, characterized in that the reproduction  
semiconductor memory is constructed of an EEPROM-type  
5 memory capable of writing electrically and erasing  
electrically, an EPROM-type memory capable of writing  
electrically and erasing by ultraviolet ray, a fuse ROM-  
type memory, a SRAM-type memory, a SRAM-type memory or  
DRAM-type memory backed up with a battery, or any of the  
10 combinations of the memories.

69. A method of sound recording and reproduction  
using a recording and reproduction system as described  
in Claim 10, characterized in that the digital memory  
recorded with information is configured of at least a  
15 semiconductor memory, an optical disk, a magnetic disk,  
a digital audio tape or the like large-capacity storage  
means including an EEPROM-type memory, an EPROM-type  
memory, a fuse ROM-type memory, a SRAM-type or DRAM-type  
memory backed up with a battery, or any of the  
20 combinations of the memories.

70. A method of sound recording and reproduction  
using a recording and reproduction system as described  
in Claim 11, characterized in that the sound recording  
and reproduction digital memory is configured of at  
25 least of a semiconductor memory, an optical disk, a  
magnetic disk, a digital audio tape or the like large-  
capacity storage means.

1 3. Detailed Description of the Invention

Industrial Field of Utilization

The present invention relates to a recording and reproduction system with a sound recording section and a reproduction section thereof separated from each other, or more in particular to a recording and reproduction system achieving the reduction in size and weight of the reproduction section with an improved method of transferring a digital signal from a sound recording section to a reproduction section while assuring an efficient storage.

[Prior Art]

First, a recording and reproduction system of a conventional construction will be explained for the understanding of the basic functions of the present invention. Conventionally, a recording and reproduction system uses a sound recording method shown in Fig. 2.

This drawing is described in JP-A-63-189296 and represents a method of writing audio information with the sound recording side (writing equipment side) and the reproduction side (card side) separated from each other. The writing into the reproduction side is controlled at the sound recording section on the write equipment side. The memory of the reproduction section is made up of an EPROM, and the data transfer is for converting a parallel into a serial signal. After conversion, the serial signal is converted into a parallel signal and is written into the EPROM. Also,

1 there is provided a power terminal for EPROM write pulse.

A write address for this system is generated with reference to a clock source from the write side, and is stored with the A/D converter and the RAM in synchronism with each other. Also at the time of reproduction, serial transfer is effected at a similar speed, and the signal is written into the EPROM after parallel signal conversion. According to this proposal, there are provided two circuits of address generator. One of them is for generating an access timing to convert the serial signal into a parallel signal and write into the EPROM, and the other for generating an address timing for reproduction. Especially, a comparatively small-scale sound recording and reproduction system is proposed for transferring all the contents of the RAM on the recording side to the EPROM.

On the other hand, as described in JP-A-61-284898, there is proposed a method of reproducing the recorded desired audio information as a recording-reproduction integrated type. According to this proposal, there is provided a RAM of the head address storage section separately from the storage section of audio information, and it is possible to set and display a head address by selector means of a track-designating switch for designating a head address.

[Problem that the Invention is to Solve]

1           The problem of the prior art mentioned above  
first lies in that in the recording/reproduction-  
separated type, no address is set for each audio file at  
the time of transfer and writing. As a result, all the  
5 contents of the RAM are transferred to the EPROM. Also,  
in the case of writing into the EPROM, it is necessary  
to initialize (clear) with ultraviolet ray or the like  
each time. Therefore, according to this proposal, a  
long time is required for transferring or clearing all  
10 the audio information.

          The second point is that due to the integrated  
type but not the recording/reproduction-separated type,  
the head address of each audio file is stored and the  
particular address is used as an object of search. As a  
15 result, the problem mentioned below is posed when the  
memory is increased to large capacity. First, because  
there is one memory for recording and reproduction, all  
the contents recorded are stored. Thus, the required  
audio information is determined and stored at the time  
20 of recording, or the head address is selected and heard  
at the time of reproduction. Another problem is that  
the mechanism of accessing the audio file requires a  
long time for setting the address counter of the large-  
capacity memory, and that the clearing of the audio  
25 information takes a long time as all the memories are  
required to be cleared. The former requires a large  
capacity of the memory in the case where a great amount  
of information is involved, thereby posing a special

1 problem in a portable-type system. The latter, on the  
other hand, poses a problem in the case of a large  
capacity, and is suitable for a system of a compara-  
tively small capacity.

5           Accordingly, the basic object of the present  
invention is to provide a recording and reproduction  
system large in capacity in total terms, wherein in the  
case where the sound recording section and the reproduc-  
tion section are separated from each other, the sound  
10 recording section is increased in capacity to store a  
great amount of audio information, the information is  
extracted as desired for each audio file, transferred  
and written into the reproduction section of a compara-  
tively small capacity, and the initialization time for  
15 writing is shortened by increasing the speed of the  
memory-clearing time.

[Means for solving the Problems]

          According to an embodiment of the present  
invention, the object mentioned above is achieved in the  
20 manner mentioned below.

          First, the sound recording section has a  
plurality of index address registers. Further, the  
reproduction section is configured to have a plurality  
of head address registers each as a pair with the index  
25 address register. Also, the contents thereof are  
configured of a memory of content address type, for  
example, which is capable of searching for coincidence.  
Further, there is provided a sound presence/absence flag

1 bit as a pair with the two registers. In the final  
stage of the full audio file transfer, on the other  
hand, the index register for reproduction memory is set  
to the maximum value of the register, for example. As a  
5 result, the absence of an audio file can be designated  
in the transfer thereof.

By the configuration described above, a  
multiplicity of audio files on the sound recording side  
are extracted as desired and transferred and written in  
10 the reproduction section, so that the reproduction  
memory converts and stores as successive addresses the  
addresses of discrete audio files. Also, the time for  
extraction of the audio file at the time of transfer/  
writing and reproduction can be shortened because of the  
15 use of the memory of content read type. Further, the  
sound presence/absence flag bits added to the index  
address register and the head address register set the  
presence of audio information in the audio file to "1"  
and the absence thereof to "0", for instance. As  
20 result, all the audio information is hypothetically  
cleared in the audio file of the reproduction section by  
setting all the flags to "0". Thus the initialization  
time before writing into the reproduction memory is such  
as to remarkably increase the clearing speed since the  
25 clearing is made by the number of the registers of the  
reproduction section, i.e., the number capable of being  
stored in the audio file.



1           As explained above, the recording and repro-  
duction system according to the present invention is  
such that a given audio file recorded in the sound  
recording section is stored by being written into the  
5 reproduction section thereby to achieve a high speed of  
clearing or shortening of the clearing time.

[Operation]

          At the time of transfer and writing, the sound  
recording control section is activated by a transfer  
10 instruction inputted at the sound recording operating  
section, so that the index address of the audio file  
extracted as desired is set in the address counter and  
is transferred from the sound recording section to the  
reproduction section. At the sound recording section,  
15 with the particular address as an initial value, the  
address counter generates an address of the sound  
recording memory, and the audio information is read out.  
At the reproduction section, the head address register  
of the audio file is set by the transfer of the index  
20 address. In the first audio file, the address 0, for  
instance, of the reproduction memory is stored as a head  
address. At the head address of the next audio file, on  
the other hand, the final value of address +1 of the  
address counter of the first audio file is stored. In  
25 this way, each time the audio file is transferred, the  
head address register is sequentially set. As a result,  
as to the index address of a given audio file of the  
sound recording side, the audio file which is processed

1 at the reproduction memory and dissipated at the sound  
recording memory is continuously written. By the way,  
the information is a digital signal and therefore can be  
transferred at high speed.

5 The selection of the index address of the  
reproduction section and the head address value of the  
audio file is effected by the content address memory,  
and therefore the search therefor is high in speed.  
Also, both the index address of the audio file and the  
10 head address become the object of search, and the  
selection thereof is set at the position of the audio  
file at the original sound recording memory or the  
reproduction memory.

Further, as to the presence or absence of the  
15 sound, the state is stored in the sound presence/absence  
flag bit added to the head address register mating with  
the index address register, and therefore only the  
particular part may be erased for clearing the sound.  
As a result, the clearing time of the recording and  
20 reproduction system according to the present proposal is  
shortened for higher speed than when all the memories  
having the audio information is cleared in the prior  
art.

Also, in view of the fact that the sound  
25 presence/absence flag bit is available for clearing  
control for each audio file, it possible to clear  
individual audio files by the sound presence/absence  
flag bit in addition to the clearing of all the files.

1           As a consequence, the clearing operation can  
be implemented at high speed with a very simple  
configuration without erasing all the files unlike in  
the prior art.

5           By the way, the sound recording memory is  
comprised of a semiconductor memory, an optical disk, a  
magnetic disk, a digital audio tape or the like large-  
capacity storage device. As a result, the sound  
recording section can manage and store the sound  
10 recording data collectively in large amount in various  
fields of the user hobby including classic music and  
various stories. thus the sound recording section  
making up a large capacity is realized as a system in  
the free-standing form or semi-portable free-standing  
15 form.

The reproduction memory, on the other hand, is  
configured of an ordinary semiconductor memory device,  
such as an EEPROM-type memory cell written electrically  
and erased electrically, an EPROM-type memory cell  
20 written electrically and erased by ultraviolet ray, a  
fuse ROM-type memory cell, a SRAM-type memory cell, a  
SRAM-type memory cell backed up with a battery, a DRAM-  
type memory cell or any combination of these memories.  
The reproduction section, whose reproduction memory may  
25 be small in capacity as compared with the ROM or RAM of  
the sound recording memory, is easily integrated into a  
chip with the control section. As a result, the size

1 can be reduced in package level, thus realizing a reproduction section of card or pocket size.

Accordingly, the reproduction section becomes a compact, convenient portable device, thus realizing a recording and reproduction system with increased freedom in terms of place and time of reproduction.

The other objects and the novel features of the present invention will be clarified from the embodiments described below in detail.

#### 10 [Embodiments]

Embodiments of the present invention will be described in detail below with reference to the accompanying drawings.

Fig. 1 is a block diagram for explaining the principle of a recording and reproduction system according to the present invention. In the drawing, 2 designates a sound recording section making up a sound recording adaptor, and 4 a reproduction section made of a reproduction card accommodatable in the pocket. 6 designates an input signal inputted by way of microphone or line, and 8 an A/D conversion section including an input amplifier, a low-pass filter and an A/D conversion circuit for converting an analog input signal 6 into an audio digital signal 40. 10 designates a sound recording memory for accumulating the audio digital signal 40, 12 a sound recording control section for recording an audio file of variable size to the sound recording memory 10 or searching and controlling the audio file

1 thus recorded, and 14 a sound recording display section  
for displaying the contents thereof, and 16 a sound  
recording operating section. On the other hand, 28  
designates an output signal, and 18 a D/A conversion.  
5 section having a circuit for converting an audio digital  
signal 46 into an analog output signal 28, a low-pass  
filter and an output amplifier. 20 designates a  
reproduction memory for accumulating the audio digital  
signal. 22 designates a reproduction control section  
10 for searching the audio file transferred and stored in  
the reproduction memory 20 and controlling the  
reproduction sound. 24 designates a reproduction  
display section for displaying the contents thereof, and  
26 a reproduction operating section.  $\phi 1$  designates a  
15 clock making up a sampling frequency of the A/D conver-  
sion circuit at the time of recording an external input  
signal,  $\phi 2$  a clock for transferring the audio digital  
information from the sound recording section 2 to the  
reproduction section 4, and  $\phi 3$  a clock making up a  
20 sampling frequency for the D/A conversion circuit at the  
time of reproduction of the reproduction section 4.

On the other hand, 30 designates an audio  
digital signal, and 32 a control signal for the repro-  
duction control section 22, an index address signal for  
25 accessing the reproduction memory 20, a clock  $\phi 2$ , a  
write activation signal, etc. 34 designates a ready  
signal indicating the transfer and write standby state  
of the reproduction section 4. also, 52 designates a

1 sound recording control signal for the A/D conversion  
section 8 and the sound recording memory 10, and 54 a  
reproduction control signal for the D/A conversion  
section 18 and the reproduction memory 20. Further,  
5 130a, 132a, 134a designate connection terminals of the  
sound recording section 2, and 130b, 132b, 134b connec-  
tion terminals of the reproduction section 4.

42 designates a sound recording display  
control signal for the sound recording control section,  
10 44 an operating signal for the sound recording control  
section, 48 a reproduction display control signal for  
the reproduction control section 22, and 50 an operating  
signal for the reproduction control section.

Now, the sound recording mode described below  
15 represents an operating mode for storing an external  
audio input signal in the sound recording memory, and  
the reproduction mode an operating mode for audio output  
to an external circuit from the reproduction memory.  
Further, the transfer mode represents an operating mode  
20 for transferring audio information from the sound  
recording memory to the reproduction memory.

The sound recording control section 12 has at  
least one or more index address registers for an audio  
file, and an address counter for generating a memory  
25 address to access the sound recording memory 10. It  
controls the sound recording mode and the transfer mode.  
The reproduction control section 22, on the other hand,  
has at least one or more sets of the index address

1 register for each audio file and a head address register  
for storing an initial value of the address for  
accessing the reproduction memory 20, and an address  
counter for generating an address to access the  
5 reproduction memory 20 from the contents of the head  
address register, thereby controlling the reproduction  
mode. Specifically, the sound recording control section  
12 generates an address of the sound recording memory on  
the basis of an index address upon instruction from the  
10 sound recording operating section 16. Also, the  
reproduction control section 22 generates an address for  
the reproduction memory on the basis of an index address  
transferred from the sound recording control section.

Next, the operation of this block diagram will  
15 be explained. First, in the sound recording mode, the  
audio signal converted into an electrical signal by  
microphone at the A/D conversion section 8 under the  
control of the sound recording operating signal 44 is  
amplified to the required level by an input amplifier.  
20 Then, in order to remove the aliasing strain before A/D  
conversion, the the high frequency portions are cut off  
by the low-pass filter. After that, A/D conversion and  
digitization are effected followed by writing into the  
sound recording memory 10. This operation is performed  
25 with the clock  $\phi 1$  making up an audio sampling frequency.  
The clock  $\phi 1$  may be made variable in speed to meet  
higher requirements of precision, level, etc. of music,  
conversation, etc. By the way, the index address of the

1 sound recording memory 10 is expressed by the head address of a given audio file. Also, the index address of the sound recording memory 10 is used for searching the audio file.

5 In the transfer mode, the reproduction section 4 is connected to the sound recording section 2, and the operating signal 44 of the sound recording section is set for transfer. After that, the reproduction control section 22 is activated upon instruction from the sound  
10 recording section 12, so that the reproduction memory 20 is first cleared and becomes a write mode, while the sound recording memory 10 enters a read mode, followed by transfer of an audio digital signal. At the time of transfer, the A/D conversion section 8 and the D/A  
15 conversion section 18 are de-activated thereby to prevent the transfer from being affected while at the same time reducing electric power.

In the process, at least an address (address set as desired) extracted at the index address of the  
20 sound recording memory 10 is sequentially transferred to the reproduction memory 20 each time of transfer of the audio file of variable length, and is set in a plurality of index address registers of the reproduction memory. On the other hand, the address counter of the reproduc-  
25 tion memory 20 starts from the address zero of the audio file, and is counted up by a predetermined amount of the audio file by the clock  $\phi 2$  on the recording side. Further, at the end of the particular audio file, the



1 address on the address counter is incremented by +1, and  
is written into the head address register mating with  
the index address register. This makes up a head  
address of the next audio file. In this way, the  
5 contents of the head address register are fed back  
sequentially by the increment of the address counter,  
and index addresses which have thus far been in a given  
order are converted into continuous addresses as the  
head addresses of individual audio files of the  
10 reproduction memory 20, thus storing audio digital  
information effectively in a small-capacity reproduction  
memory 20. In this case, the index addresses and the  
head addresses are stored in all the audio files on the  
reproduction section 4 side, thus making it possible to  
15 use it for searching the reproduction memory 20 as in  
the case of the sound recording memory 10.

Next, in the reproduction mode, the audio  
digital information taken out of the reproduction memory  
20 at the D/A conversion section 18 is converted into an  
analog value at the D/A conversion circuit, smoothed at  
the low-pass filter, amplified at the output amplifier,  
and reproduced at the output unit (such as earphone) as  
an audio output signal 28. This operation is performed  
with clock  $\phi 3$  at least at the same frequency as the  
25 clock  $\phi$  for the sound recording. On the other hand, the  
sound may be heard slowly under low speed or may be  
subjected to rapid feed in the case where the clock  $\phi 3$   
is made variable in speed.

1           In the above-mentioned operating mode, the  
index address of the sound recording memory 10 is  
configured the same way as that of the reproduction  
memory 20. The address for actually accessing the  
5 reproduction memory 20, however, makes up a head address  
newly prepared at the reproduction control section. As  
a result, the memory capacity of this reproduction  
memory 20 is equal to or smaller than that of the  
address of the sound recording memory 10, and holds the  
10 relation  $M_r \geq M_s$  where  $M_r$  is assumed to be the memory  
capacity of the sound recording memory 10 and  $M_s$  that of  
the reproduction memory 20.

As explained above, according to this embodi-  
ment, the audio recording section 2 and the reproduction  
15 section 4 are separated from each other, and by trans-  
ferring an index address, an audio digital signal of a  
given address of the sound recording section 2 can be  
written into the reproduction memory 20 on the reproduc-  
tion section side. Specifically, only the required  
20 audio information may be stored partially, and therefore  
the memory on the reproduction section 4 side is econo-  
mically reduced in capacity. Also, the reproduction  
section 4 lacks a sound recording section and has a  
small memory capacity, thereby making it possible to  
25 reduce the weight and size. The object of selective  
sound recording of the audio file, on the other hand, is  
achieved even when the index address transferred from  
the sound recording section 2 to the reproduction

1 section 4 is sent by being converted into continuous  
addresses of the reproduction memory 20 in advance.

Further, even one index address register of  
the sound recording section 4 serves the purpose. Also,  
5 an address counter of presentable type may be used  
without using the register. In such a case, the desired  
address is set in the counter each time, and further the  
same address is transferred to the reproduction section  
4 as an index address. By doing so, the index addresses  
10 are sequentially stored in the reproduction section.  
Also, as for the index address register of the reproduc-  
tion memory 20, even one such register serves the  
purpose. This at least one register is used for holding  
the index address and energizing the address counter.

15 On the other hand, the signal interface means  
for the audio digital signal 30, the address and control  
signals 32, 34 may be either by cable, light or radio.  
In the case of light or radio, for example, the  
mechanical reliability of the connectors is improved for  
20 lack of a contact. 'Also, a mixed type with a cable  
power line and the other signals transmitted optically  
or by radio, is effective from the viewpoint of current  
supply at the time of sound recording transfer to the  
card 4 side. Further, in the case of cable connection,  
25 there may be considered tow types of coupling including  
the direct coupling between the sound recording section  
2 and the reproduction section 4 and the indirect  
coupling with cable extension. The form of the

1 input/output signal interface may be modified in various  
ways depending on the test environment. Also, the  
signal waveform may be shaped or otherwise similarly  
processed by a buffer amplifier or the like inserted  
5 between the input and output signals. Further, a  
divided arrangement of the power systems for the analog  
and digital system circuits is important for actuate  
operation of the circuit.

By the way, the transfer of an index address  
10 will be explained in detail later with reference to an  
embodiment.

Fig. 3 shows a second embodiment.

In the drawing, the same component parts as in  
Fig. 1 are designated by the same reference numerals  
15 respectively, and will be not described again. 8a, 8b,  
8c designate an input amplifier, a low-pass filter and  
an A/D conversion circuit respectively corresponding to  
the A/D conversion section 8 in Fig. 1. 56 designates a  
card identification circuit for recognizing the type or  
20 the inserted state of a reproduction card of the  
reproduction section 4. 58 designates a power circuit  
for the sound recording section 2, 60 a power circuit  
for the reproduction section 4, and 64 an I/O slot  
making up a socket of the sound recording section for  
25 connecting the reproduction section 4 at a connecting  
terminal in the sound recoding section 2. On the other  
hand, 18a, 18b, 18c designate a D/A conversion circuit,  
a low-pass filter and an output amplifier respectively

1 corresponding to the A/D conversion section 18 in Fig.

1. Also, 62 designates a change-over switch for the  
audio digital signal 30.

The basic operation is similar to that of the  
5 first embodiment, and therefore explanation will be made  
about the operation of the above-mentioned added circuit  
blocks.

The sound recording section 2 has the sound  
recording control section 12, the sound recording memory  
10 10, the reproduction control section 22 and the  
reproduction memory 20 activated by the sound recording  
operating signal 44. As to the audio information  
recorded in the sound recording memory 10, the repro-  
duction control signal 54 is designated in the change-  
15 over switch 62 of the audio digital signal 30. In the  
case of transfer and sound recording, the audio digital  
signal is transferred from the sound recording section 2  
to the reproduction section 4. Also, in the case of  
reproduction, the sound is outputted through the D/A  
20 conversion circuit 18a from the reproduction memory 20.

60 designates a power circuit of the  
reproduction section 4, which is configured of at least  
a primary battery or a secondary battery. In the case  
where the latter, i.e., the secondary battery is  
25 incorporated, a charging circuit is required. This  
circuit, however, may be provided in or separate from  
the reproduction section 4 or the sound recording  
section 2. The battery, on the other hand, may be of

1 exchangeable cartridge type. Further, in order to hold  
the information in the reproduction memory 20, the sound  
recording section 2 or the reproduction section 4 has at  
least a residual amount detection circuit for indicating  
5 the residual life of the battery. The battery 60 may  
have added thereto an information-holding primary  
battery adapted to be activated with the fall of level  
of an operating battery, or otherwise may be backed up  
by two-system batteries.

10               The drawing under consideration shows a  
circuit which is realizable with small size and low cost  
to the extent that the sound recording section 2 making  
up a sound recording adaptor and the reproduction  
section 2 providing a reproduction card are separated  
15 from each other and the reproduction section requires no  
sound recording function like the sound recording  
section 2. Also, since the system according to this  
embodiment is used retrieving the required information  
as desired, the sound recording section 2 is fixed and  
20 the reproduction section 4 is often carried as a  
portable type. As a result, the power circuit 58 of the  
sound recording section 2 may be supplied as an AC power  
supply. This results in the sound recording section 2  
having a large power-supplying capacity. Especially  
25 when transferring digital information from the sound  
recording section 2 to the reproduction section 4 at  
high speed, power is supplied from the sound recording  
section 2 to the reproduction section 4, whereby it

1 becomes easy, in particular, to supply large power  
required for high-speed operation of the sound recording  
memory 20. As a consequence, the power load of the  
reproduction section 4 is reduced by supplying a current  
5 from the sound recording section side at the time of  
transfer and writing. In the case where a SRAM  
including a CMOS is used as a reproduction memory, for  
instance, the current consumption of the memory  
increases substantially in proportion to the speed of  
10 frequency. One process of high-speed transfer and  
writing, therefore, becomes substantially equivalent to  
a slow reproduction of all the contents of the  
reproduction memory with normal sound speed. This  
indicates the fact that a cycle of reproduction of the  
15 contents of the full reproduction memory could be saved  
and reduced in terms of energy of the battery 60.

By the way, the power circuit 58 may have a  
battery backup function for backing up the stored  
information in the case where the reproduction memory 10  
20 is of volatile type. Also, the circuit blocks mentioned  
above are accommodated in the housings of the sound  
recording section 2 and the reproduction section 4. As  
in Fig. 1, an index address or a head address of the  
reproduction memory may be searched for as a function of  
25 the sound recording and reproduction control circuits  
12, 22. Further, the object of switching may be  
achieved also by activating the reproduction memory side  
and de-activating the D/A conversion circuit in transfer

1 mode, and by de-activating the sound recording memory 20  
on transfer side and activating the D/a conversion  
circuit at the time of reproduction, instead of by using  
the change-over switch 62.

5 Fig. 4 shows a third embodiment.

In the drawing, the same component parts as in  
Fig. 3 are designated by the same reference numerals  
respectively, and will not be described again. 70  
designates an optical disk unit for storing information  
10 by light, and 72 a buffer memory. By using an optical  
disk as the recording memory showing the drawing, the  
capacity of the sound recording memory 10 is improved  
remarkably. As a result, the portion one want to hear  
can be stored and reproduced in the reproduction section  
15 4. Also, if the optical disk unit 70 is accessed  
through the buffer memory 72, the transfer speed of the  
audio digital signal is regulated, thus facilitating the  
transfer control.

By the way, the optical disk unit has added  
20 thereto a drive circuit for read and write operation.  
Also, in place of the disk unit, a magnetic disk or a  
digital audio tape may be used with equal effect.  
Further, the buffer memory is of course effective also  
for the sound recording memory 10 using a digital audio  
25 tape, a magnetic disk or a large-capacity semiconductor  
memory of comparatively low speed in place of the  
optical disk 70. Further, the buffer memory may  
alternatively be placed on the audio input side of the



1 sound recording section 10, in which case the speed  
regulation of the sound recording memory 10 making up a  
large-capacity storage device of comparatively low speed  
and an input signal may be supported.

5 Fig. 5 shows a fourth embodiment.

In the drawing, the same component parts as  
those in Fig. 3 are designated by the same reference  
numerals, and will not be described again. 74  
designates a transmission circuit for converting a  
10 parallel signal of the audio digital signal 30 to a  
serial signal and modulating the same signal into an  
electric wave, and 76 a transmitting antenna thereof.  
54' designates a reproduction control signal group for  
controlling the change-over switch and the D/A  
15 conversion circuit 18c and also controlling the  
transmission circuit 74. On the other hand, 78  
designates a receiving antenna, and 80 a receiving  
circuit for receiving a transmitted electric wave and  
converting an audio digital signal making up a serial  
20 signal into a parallel signal and modulating the same  
signal. 18c' designates a D/A conversion circuit, 18b'  
a low-pass filter, and 18a' a D/A conversion section  
including an output amplifier for converting an audio  
digital signal converted into a parallel signal, into an  
25 analog audio output signal 28'. Also, 90 designates a  
wireless receiver configured of the above-mentioned  
circuits.

1           As shown in the drawing, by converting the  
audio digital signal directly into an electric wave, the  
resistance to external noises is strengthened as a  
result of conversion of an analog signal to electric  
5 wave. Also, in the case where the audio digital signal  
30 is transferred from the sound recording section 4 in  
the form of serial signal, the transmission circuit 74  
is not required to convert a parallel into a serial  
signal.

10           In this way, a compact reproduction section 4  
can be accommodated in the packet, bag or the like, and  
further the reproduced sound can be heard by a compact  
wireless receiver 90 with an output of the reproduction  
section 4, thereby improving the convenience and the  
15 operability. By the way, the reproduction section 4 may  
be controlled bidirectionally on the wireless receiver  
90 side thereby to select a given sound at the receiver  
90. Also, although the wireless receiver 90 is plotted  
in a square in the drawing, the shape may be modified in  
20 any manner to meet the requirement of engaging the ears  
directly.

A fifth embodiment is shown in Fig. 6.

In the drawing, a circuit is shown in which  
the D/A conversion section 18 including the D/A  
25 conversion circuit 18c of the reproduction section 4,  
the low-pass filter 18b, the output amplifier 18a, etc.,  
is eliminated from the system of Fig. 5, and the  
reproduction is effected by the wireless receiver 90.

1 By doing so, the reproduction section 4 can be further  
reduced in size and weight as compared with the system  
shown in Fig. 4.

A sixth embodiment is shown in Fig. 7.

5 In the drawing, a system is shown in which the  
A/D conversion section 8 of the sound recording section  
4 is eliminated from the system of Fig. 3, 100  
designates a non-volatile semiconductor memory. This  
non-volatile memory 100 may use at least a memory device  
10 with audio information written externally, such as an  
EPROM for writing electrically and erasing by ultra-  
violet ray, an EEPROM for writing and erasing elec-  
trically, a SRAM backed up with a battery, a DRAM or the  
like.

15 A seventh embodiment s shown in Fig. 8.

In the drawing, a system is shown from which  
the A/D conversion section 8 (8a, 8b, 8c) of the sound  
recording section 4 is eliminated. In this case, the  
memory 100' uses a large-capacity storage device such as  
20 an optical disk, a magnetic disk, a digital audio tape  
or a comparatively low-speed semiconductor memory in  
which audio information is written externally.

The sixth and seventh embodiments mentioned  
above can reduce the number of circuit components of the  
25 A/D conversion section 8 from the sound recording  
section 2, and therefore the housing of the sound  
recording section 2 can be reduced in both size and  
weight.

1                   Next, an eighth embodiment is shown in Fig. 9.

                  This embodiment of the invention will be explained in detail below with reference to the accompanying drawing. In the drawing, the same component parts as those in Fig. 3 are designated by the same reference numerals respectively, and will not be described again. 138 designates an index address register for storing a head address of an audio file of the sound recording section 2. This register includes at least one register unit. Also, 140 designates an index address register for storing an index address of the same audio file of the reproduction section 4, 142 a head address register for storing a head address of an audio file of the reproduction memory 20, and 144 a flag bit for indicating the presence or absence of a sound. These form a table in pairs of the index address register 140, the head address register 142 and the flag bit 144, and make up at least one pair. Also, 12a designates a control circuit in the sound recording section 12, 12b an index address register, and 12c an address counter. The counter 12c is supplied with a sampling frequency, that is, the clock  $\phi 1$  or the transfer clock  $\phi 2$  in sound recording and transfer modes respectively for counting up. On the other hand, 22a designates a control circuit in the reproduction control section 22, and 22b a register table configured of a head address register 142 and flag bit. 22c designates an address counter, which is supplied with the clock  $\phi 3$

1 or the transfer clock  $\phi 2$  in the reproduction and  
transfer modes for the purpose of count-up respectively.  
110 designates a clear energization signal, 32a an index  
address signal, 32b a control signal for the control  
5 circuit 22a of the reproduction control section 22, and  
32c a refresh demand signal for the DRAM used with the  
reproduction memory 20. Also, 34 designates a ready  
signal indicating the write standby state of the  
reproduction section 4.

10 On the other hand, 52a designates an address  
signal for the sound recording memory 10, 52b a memory  
control signal for the sound recording memory 10, 52c an  
activation signal for the A/D conversion circuit 8c, 54a  
an activation signal for the D/A conversion circuit 18c,  
15 114 an index address setting signal, 116 a counter  
activation signal for transferring an index address and  
setting for activation of an initial value of the  
address counter, 118 a signal for sequentially  
designating and setting the index address signals 32a  
20 from the sound recording section 2, and 120 a counter  
activation signal for activating (energizing) the  
initial value of the address counter 22c on the basis of  
an index address. Also, 122 designates an address  
counter feedback signal for feeding back the contents of  
25 the address counter 22c to the index register.

Further, 138 designates an index address  
register for storing a head address of an audio file of  
the sound recording section 2, and is comprised of at

1 least one register unit. Also, 140 designates an index  
address register for storing an index address of the  
audio file in the reproduction section 4, 142 a head  
address register for storing a head address of the audio  
5 file of the reproduction memory 20, and 144 a flag bit  
indicating the presence or absence of the sound. These  
are formed in a table in pairs of the index address  
register 140, the head address register 142 and the flag  
bit 144. These components are configured of one or more  
10 pairs.

The operation of this embodiment will be  
explained below. The writing of audio information in  
the sound recording memory 10 of the sound recoding  
section 2 and the reproduction from the reproduction  
15 section 4 shown in the drawing are effected in the same  
way as in the first embodiment. Therefore, the  
operation flow shown in Fig. 10 for the operation of  
transfer and writing into the reproduction section 4  
from the sound recording section 2 and the state of the  
20 index address, the head address and the flag bit of the  
table managing the variable-length audio file will be  
explained with reference to a specific example shown in  
Fig. 10-1. By the way, the address sizes of the system  
are assumed to include 64 G bytes (36 bits in the number  
25 of addresses) in the memory capacity of the sound  
recording section and 4 G bytes (32 bits in the number  
of addresses) in the memory capacity of the reproduction  
section.

1           First, the sound recording into the  
reproduction section 4 is effected in such a manner that  
the reproduction section 4 is inserted into the sound  
recording section 2, and after that, at least given one  
5 of the index addresses (36 bits) of the audio file is  
extracted from the sound recording operating signal 44,  
and (000---000000011) is inputted as shown in the binary  
indication of the case (2) of Fig. 10-1, thereby  
designating a write demand for write activation of the  
10 reproduction memory 20. As a result, the write demand  
is turned on, the clear circuit 110 is energized, and  
the reproduction memory 20 and the address counter on  
the reproduction section side are initialized by the  
designation from the clear start signal 112. Further, a  
15 ready signal 34 indicating a write standby state is  
returned to the sound recording section 2. In the next  
step, the sound recording section 2 side sets the  
address counter from the index address signal, while the  
reproduction section 4 side sets the index address  
20 register of case (2) through the index address signal  
32a, and further the address 0 (case (s1) in Fig. 10-1)  
as a head address. By the way, the head address is not  
confined to this address 0, but may be set a a head  
address of the first audio file for 0 and subsequent  
25 addresses. Next, the digital information of the audio  
file is transferred, during which the refresh signal 32c  
of the DRAM is demanded from the sound recording section  
2 side. By the way, the counter mounted on the

1 reproduction section 4 is used as a refresh counter.  
The transfer of the audio signal and the demand for  
refreshing are repeated under the rules of signal  
transfer, so that the next audio file designated as an  
5 index addresses (case (3) in Fig. 10-1) is repeatedly  
transferred in a similar process. In the process, the  
figure of the final value +1 of the address counter of  
the previous audio file (case (s2) in the same drawing)  
is set in the head address of the reproduction memory  
10 20. Also, the detection of the end for each file is  
generally decided by the entry of the flag bit of the  
next audio file.

Further, after the transfer of a predetermined  
number of audio files is completed, the process of  
15 transfer completion is effected. As shown in case (s5)  
of Fig. 10-1, for instance, the completion is designated  
by transferring the maximum value (111---111111111) of  
the index address from the sound recoding section 2 to  
the reproduction section 4. Also, in response to this  
20 maximum value, the sound presence/absence flag 144 of  
the reproduction section 4 stores "0", for example. As  
a result, it is decided that subsequent audio files are  
absent (lacking the audio information). By the way,  
this decision is possible also by detecting the maximum  
25 value of the index address. In the reproduction  
process, on the other hand, the above-mentioned table  
contents form a basis. When case (s2) is designated  
from the reproduction operating section, for instance,



1 the value of the head address register (00---0001001) is  
set in the address counter, so that the address of the  
reproduction memory 20 and the sound are outputted.  
Further, the operation is stopped immediately before by  
5 observing the "1" state of the sound presence/absence  
flag of the next file (00---00010001). Also, in the  
repeat operation between the first (case (s1) in the same  
drawing) and the last (case (s4) in the same drawing) of  
the audio file, the repeat address of (000---00000000)  
10 is used in binary notation for starting the operation,  
and the address of (000---00110111) immediately before  
the head address (case (s5) in the drawing) mating with  
the maximum value of the index address for ending the  
operation.  
15 On the other hand, since the last value of the  
sound recording section 2 is stored in case (n+1)  
following the initial value of the last audio file  
indicating in case (n) as the n-th audio file stored in  
advance in the sound recording section 2, the end of the  
20 audio file can be determined.

After this transfer completion process, the  
demand for writing the audio file is turned off, and the  
pull off the reproduction section 4 is permitted.  
Further, since the reproduction section 4 is separated  
25 from the sound recording section 2, the refreshing of  
the DRAM is shifted to the self-freshing state in the  
reproduction section 4 side, thereby holding the stored  
information. By the way, in order to assure transfer,

1 the reproduction section 4 or the sound recording  
section 2 may have added thereto a display function for  
indicating that the system is in writing process or the  
contents of the audio file on the reproduction section  
5 4. Further, for confirming the contents thus  
transferred, the reproduction may be made under  
insertion or pulled-off state.

Next, the processing of clearing the stored  
information in the reproduction section will be  
10 explained. The sound presence/absence flag bit 1434 is  
configured of an index address register 140 indicating  
the initial value for each audio file and a head address  
register 142 of the audio file of the reproduction  
memory 4 in pair. For this reason, in the case where  
15 all the audio files are set to "0", for example, it is  
decided that the state is that no audio file is  
contained in the reproduction memory, i.e., that the  
file is cleared. Also, the flag bit is capable of  
clearing each audio file. In such a case, the next  
20 audio file may be called immediately on the assumption  
that there is no audio file cleared. In the other case,  
the counting of the address is advanced chronologically,  
all the inputs of the D/A conversion circuit are fixed  
to "0" or "1". Alternatively, the output amplifier 18a  
25 is controlled to create a voice interval.

The former makes up memory redundant means of  
a kind for avoiding an error bit or the like generated  
in the audio file since the next audio file is accessed.

1 As a result, defective bits can be saved for each  
variable-length audio file. In this creation of a voice  
interval due to the flag bit of "1", it cannot be  
decided that the audio file is ended. In view of this,  
5 the last value of the stored information may be decided  
by the maximum value of the index address register, or  
for example, by (111---11111111) of case (s5). One of  
flag bits may also be added for redundancy.

By the way, in the case where all the bits of  
10 the reproduction memory 20 are bot cleared, the address  
counter 22c may be written after scanning all the  
addresses of the memory 20 by setting the audio digital  
information making up an input to the memory 20 to at  
least "0" or "1". Also, even when the clear circuit 110  
15 is located on the sound recording section 2 side instead  
of on the reproduction section 4 side, the instruction  
for clearing it is possible.

On the other hand, a clear mechanism may be  
employed also for the sound recoding section 2. In that  
20 case, the sound presence/absence flag bit is added to  
each index address register to manage the flag condi-  
tions. Also, the attribute of the audio file such as  
conversation, music, etc. may be separated by adding the  
flag of the sound recording section 2 and the reproduc-  
25 tion section 2. Such a flag may be used to make  
variable the sampling frequency, i.e., the clocks  $\phi 1$ ,  
 $\phi 3$ . By doing so, the sampling frequency of the sound  
including music can be increased in speed, thereby

1 giving rise to the realization of a reproduced sound of  
higher quality. Also, in conversation, the sampling  
frequency may be reduced in speed to save the memory  
consumption. Further, as an effect of a flag bit, the  
5 sequential number of a file can be determined by  
detecting and counting flags "1", for example. Also, the  
file setting such as search for the lead in an audio  
file is made possible by setting the count as described  
above. Furthermore, after detection of the flag "0",  
10 the power consumption at the reproduction section 4 can  
be saved except for the repeat operation. This is  
achieved by set the information-storing reproduction  
memory 2 in standby state and de-activating the  
remaining circuits for preventing battery consumption.  
15 A standby state capable of rising is also recommended.  
In addition, the reproduction section 4 may be provided  
with a sleep mode and deactivated or rendered into  
standby state by low power consumption as described  
above after a predetermined period of detection of the  
20 end of the sound.

By the way, the residual amount of the  
reproduction memory 20 may be determined by subtracting  
the head address value indicated in (case (s5) in Fig.  
10-1) or the last address of the reproduction memory 20,  
25 for example. As for the residual amount of the sound  
recording memory 10, by contrast, the last value of the  
audio file is stored at the end. Subtraction is  
therefore made in similar fashion from the last value of

1 the index address. Also, that the end of each audio  
file is involved in the above-mentioned case is  
indicated by the transfer of the index address of the  
next audio file. This may be replaced by the operation  
5 in which the number of clocks  $\phi 2$  transferred from the  
sound recording control circuit 12a to the reproduction  
control circuit 22a is transferred to and controlled by  
the amount of audio files. The resulting count of  
clocks may be used as a unit of audio file amount.

10 A ninth embodiment is shown in Fig. 11.

In the drawing, 22b' designates a register  
table, 140' a register for storing the index address of  
the audio file, 142' a register for storing a head  
address of the audio file mating with 140', and 146 a  
15 file flag bit indicating the state at a block of the  
audio file.

The system shown in the drawing, unlike that  
shown in Fig. 10-1, is such that the audio information  
is controlled by blocks. The contents of the register  
20 table for storing the reproduction memory in divided  
form in order to manage the audio information by blocks  
unlike in Fig. 10-1 are shown in the drawing. The flag  
bit 146, for example, as in case (1) of the same  
drawing, has "01" indicating the start of the head block  
25 of the audio file. As in case (2), "10" indicates an  
intermediate block of the audio file. As seen from case  
(4), "11" indicates the ending block of an audio file.  
Also, "11" indicates the ending block of an audio file.

1 On the other hand, "00" at and after case (n-5)  
indicates the absence of an audio file in the block,  
corresponding to the sound presence/absence flag in "0"  
state shown in Fig. 10-1.

5 In the drawing, the address sizes are such  
that the capacity of the sound recording memory 10 of  
the sound recording section 2 is assumed to be 64 G  
bytes, and that of the reproduction memory 20 of the  
reproduction section 4 to be 4 G bytes. Also, the index  
10 address register 140', in order to manage the reproduc-  
tion memory 20 in blocks, has the unit capacity thereof  
divided into 4 M bytes. As a result, the size of the  
index address is 14 bits. This is similar to the case  
of the sound recording memory. On the other hand, the  
15 head address register, which manages the reproduction  
section in blocks in similar fashion, is 4 M bytes in  
capacity, with the address size of ten bits. As a  
result, the capacity of the register table 22b' for  
divided storage is  $2^{10}$  bits along word and 26 bits along  
20 bit. These values correspond to the memory capacity of  
about 64 K bits assuming a cell area 2.5 times larger  
than the general-purpose SRAM in the case of using a  
content address memory as a table. As a result, the  
table capacity is as small as less than five digits of  
25 the reproduction memory 20, which is a very small figure  
as compared with that of the reproduction memory 20.

Also, the last block of the audio file is  
designated by the maximum value (11111111111111) of the

1 index address register as in the case of Fig. 10-1. In  
the drawing, case (n-6) providing the end of the audio  
file i makes up the last block containing audio informa-  
tion. The head address register 142', on the other  
5 hand, as shown in (n-5) and subsequent cases, has the  
count-up thereof stopped. The block management of the  
reproduction memory 20 has a secondary effect mentioned  
below. With the flag bit detecting the start "01", for  
instance, the search, high-speed retrieval, etc. of the  
10 audio file are made possible. Also, by counting the  
block "00" lacking information of the audio file, the  
residual amount of the blocks can be checked. Further,  
it is possible to determine the sequence of the file  
from the number of the count of the start "01", and the  
15 selection of the audio file can be set by the number of  
count. Furthermore, the result of detection of "00" may  
be used for reduction of power consumption as in the  
case of Fig. 10-1.

By the way, the check of the residual amount  
20 may also be implemented, as in the aforementioned  
embodiment, by subtraction of the maximum value of the  
head address register and the value of the head address  
of the audio file, say, the value of (case (n-5) in  
Fig. 11).

25 The memory used for the register tables 22b,  
22b' in Fig. 10-1 or Fig. 11 may be a general-purpose  
memory rather than the content read memory capable of  
searching collectively. In such a case, the unit

1 register contents along the word are sequentially read,  
and cyclically searched for coincidence in table  
contents. Fig. 12 shows a tenth embodiment.

In the drawing, the same component parts as  
5 those in Fig. 1 or 3 are designated by the same refer-  
ence numerals respectively, and will not be described  
again. This drawing shows a specific example of the  
sound recording section 2 and the reproduction section  
4. The sound recording section 2 stores external analog  
10 information in the form of digital information.  
Further, a desired audio file is selected from the sound  
recording operating section 16 and the sound recording  
display section 14, and transferred and written into the  
reproduction section 4, which in turn selects and  
15 reproduces the contents recorded as desired. In the  
aforementioned reproduction, the reproduction for each  
file, the continuous reproduction in a designated range,  
the reproduction of a plurality of designated files,  
etc. can be effected by detecting the head address or  
20 the sound presence/absence flag bit next to the audio  
file in the reproduction memory 20.

The reproduction operating section 26 performs  
such operations as inputting an index address of the  
audio file, starting, stopping or repeating the repro-  
25 duction, setting the reproduction range or reproduction  
sound output level, or clearing the reproduction memory  
20. Also, the reproduction display section 24 displays  
the index address of the audio file inputted for



1 reproduction. It may also display "under display", the  
residual life of the battery, the audio output level,  
etc. The sound recording operating section 26 and the  
sound recording display section 24 of the sound record-  
5 ing section 2, on the other hand, may perform the  
operation or display at least similar to the reproduc-  
tion operation in order to record the sound in the sound  
recording memory 10 or to transfer the storage informa-  
tion to the reproduction memory 10.

10 By the way, the designation or search of the  
audio file is expressed by binary notation of the index  
address in the cases mentioned above. In spite of this,  
numerals or file names easy to understand are readily  
used. This is also the case with the head address.

15 Further, in view of the fact that the housing  
of the reproduction section 2 has the insertion section  
thereof into the sound recording section, constructed of  
an almost evenly flat surface having no adverse effect  
on insertion or a surface with an uneven slot as an  
20 insertion guide, the reproduction section 2 can be  
inserted or pulled off smoothly. Also, the overlapped  
portions between the sound recording section 2 and the  
reproduction section 4 may be displaced from the  
arrangement of the display section 24 or the input  
25 operating section 26 of the reproduction section 4, in  
order to permit the operation with the reproduction  
section 4 loaded. Also, the operating section 26 and  
the display section 24 may be displaced from the

1 overlapped portions to contribute to a flat-surface  
configuration.

Fig. 12-1 shows an eleventh embodiment.

In the drawing, the same component parts as  
5 those in Fig. 1, 4 or 12 are designated by the same  
reference numerals respectively, and will not be  
described again. 200 designates a small-size memory  
processing unit for memory card, IC or the like. This  
embodiment represents a recording and reproduction  
10 system of parent, child and grandchild type for adding  
functions to the reproduction section 4 or providing  
additional memories.

As a form of application of the system shown,  
for example, a desired audio file is selected from the  
15 sound recording display section 14 and the sound  
recording operating section 16 of the sound recording  
section 2 which is a parent, information is transferred  
and written into the reproduction section 4 as large as  
an "electronic notebook" as a child, and the same  
20 information is recorded in a small memory card or IC  
card as a grandchild. The contents thus recorded can be  
shared with other electronic notebook, etc. Also, it  
may be possible to provide audio information, a proces-  
sing program, etc. in the form of memory card or IC card  
25 on the part of the manufacturer or software development  
maker. Further, by adding optional functions such as  
wording of a sound to the reproduction section 4, it  
becomes possible to store sentences in a memory card.

1 By the way, the card acting as a grandchild is not  
confined to the one using a semiconductor memory, but  
may take a form of medium like various optical or  
magnetic disks or the like of very small size.

5 Fig. 12-2 shows a twelfth embodiment.

In the drawing, the same component parts as  
those in Fig. 1, 4 or 12 are designated by the same  
reference numerals respectively, and will not be  
described again. 210 designates a speaker, and 16' an  
10 operating section for performing the recording and  
reproduction. The sound recording section 2 also  
represents a device capable of sound reproduction. For  
example, the sound recording section 2 is a multi-  
function sound recording and reproduction device having  
15 at least such functions as FM, AM, TV, radio, optical  
disk, magnetic disk, digital audio tape and time-  
reserved recording. By adding this device to the  
recording and reproduction system according to the  
present invention, application to multi-media is  
20 promoted and expanded.

According to this system, the reserved  
recording function is utilized in such a manner that  
while one is asleep, audio information can be recorded  
in the large-capacity storage means of the sound  
25 recording memory 10, and further, all the contents  
selectively written or newly recorded among them are  
transferred and written. The transfer to the reproduc-  
tion section 4 is high in speed due to digital

1 recording. For the capacity of 128 M bits, for example,  
the reproduction of about 35 minutes is possible with a  
sampling frequency of 8 kHz, on the assumption of using  
an 8-bit quantization for the A/D conversion section 8  
5 and the D/A conversion section 18 with an uncompressed  
sound. In digital recording, only the time as short as  
1.7 seconds is required for completion in the case of  
the transfer cycle of 100 ns. The large current for the  
memory consumed at the time of high-speed transfer is  
10 supplied from the sound recording section 2 at the time  
of loading the sound recording section 2 and the  
reproduction section 4, and therefore poses no problem.  
The contents recorded in this connection may include  
various items such as conversation, story, English  
15 conversation, stock or other business information, or  
leisure or hobby. Thus they are used in areas where the  
sound quality is paid comparatively small attention. In  
the case of music which emphasizes the sound quality, by  
contrast, the sampling frequency, or the number of  
20 quantization bits of the A/D conversion section 8 or the  
D/A conversion section 18 is increased. For the  
capacity of 4 G bits of the reproduction memory 20, for  
instance, a music as long as about 1.7 hours can be  
enjoyed in the case of 16-bit quantization with an  
25 uncompressed sound at the sampling frequency of 44.1  
kHz. In the case where a long-time reproduction is  
realized in this way, several musics may be stored, and  
any of them, such as "XXXX" in the first movement or

1 "YYYY" in the fifth movement of a classic music, may be  
heard by retrieval as desired.

The sound recording section 2 may of course be  
formed as either free-standing or portable type or  
5 modified as desired to meet the environmental require-  
ments. It is also possible to introduce a recording and  
reproduction system according to the present invention  
in telephone or the like to acquire a great amount of  
information with automatic answering and recording  
10 function.

As explained above, according to the present  
invention, the amount of semiconductor memory is  
utilized effectively to store a sufficient amount of  
audio information desired by the user with a small  
15 memory capacity. This is attained by storing audio  
information from the sound recording section 2 to the  
reproduction section 4 sequentially and continuously in  
the form of content index. Further, since the index  
address is also stored in the sound recording section 2  
20 and the reproduction section 4, the audio file number on  
the sound recording section 2 side can be transmitted  
directly to the reproduction side. As a result, the  
reproduction side can be accessed for search with the  
same number as on the sound recording section 2. Also,  
25 since access for search is possible with the head  
address of the reproduction side, the audio file can be  
handled easily at the time of reproduction. By the way,  
although the embodiments described above do not show any

1 method of searching the contents of recorded informa-  
tion, high-speed information search is possible by  
providing an information search circuit in the sound  
recording section anew on the output side of the sound  
5 recording memory to read the sound recording memory at a  
speed as high as in high-speed mode. The reproduction  
section, on the other hand, is a circuit similar to the  
sound recording section, and is capable of reading  
slowly with the clock  $\phi 3$  providing a sound speed. Also,  
10 a new high-speed clock may be provided for high-speed  
search. Further, the transfer clock  $\phi 2$  may be used with  
the sound recordnig section and the reproduction section  
loaded.

In the case where the audio file is reproduced  
15 from the head address, on the other hand, the storage  
information may be difficult to hear for lack of the  
head of the reproduced sound. In order to obviate this,  
an address subtractor function may be added to repro-  
duce from several steps before the head address of the  
20 audio file. Also, a rapid feed, which is attained  
simply by increasing the speed of the clock  $\phi 3$  for  
reproduction, is easily realized. In similar fashion,  
in the case where reproduction is made in the sound  
recording section 2, the above-mentioned functions for  
25 sound reproduction may be provided. Further, there may  
be provided at least one bit of space between adjacent  
audio files for transfer and writing. This period may  
be used for various processings including the feedback

1 from the address counter of the head address next to the  
audio file.

By the way, the present invention is not  
limited to the above-mentioned embodiments. The outline  
5 of the system or the method of storing audio signals,  
for example, may be modified in various ways according  
to the application. Also, the operating sequence may be  
modified, so that in erasing the information, for  
instance, an erroneous erasure can be prevented by a  
10 confirmatory execution on the display section. Also,  
the operability is improved by operation with menu  
display. As an example, a touch-type input may be  
employed with the display section and the operating  
section integrated with each other. Further, although  
15 the compression or non-compression of audio information,  
bit width or the like is not specifically referred to in  
this embodiment, the number of quantization bits of the  
A/D conversion circuit or the sampling frequency, i.e.,  
the clocks  $\phi 1$ ,  $\phi 3$  may be determined in accordance with  
20 the condition of sound recording and reproduction of an  
audio signal. The clocks may be set either by digital  
selective setting or analog variable setting of the  
frequency.

On the other hand, there may be provided a  
25 plurality of reproduction sections 4. In such a case,  
all the contents written in the reproduction section may  
be identical or different from one to another. The  
latter may be realized, for example, by adding such a

1 flag bit as to correspond to the number of a reproduc-  
tion section 4, to the index address register of the  
sound recording section 2.

Further, the above-mentioned contents may be  
5 strictly controlled by utilization of a microprocessor  
or the like, thereby realizing an easy-to-operate high-  
performance recording and reproduction system.

In the aforementioned embodiments, the direct  
transfer and writing of an audio digital signal has been  
10 explained. As an alternative, however, the digital  
signal may be converted into an analog signal before-  
hand, followed by digitization and writing. In such a  
case, the sound quality is deteriorated, but the other  
features of the invention are actively utilized. Also,  
15 a sensor instead of microphone may be used in a sound  
recording and reproduction of all types having a sound  
intensity including the heart throb or environmental  
noises or in a data recording system for storing in  
digital form an analog value changing with time such as  
20 temperature or humidity.

Furthermore, audio information of the repro-  
duction section 4 may be received at one sound recording  
section and transferred to another sound recording  
section depending on applications involved. In such a  
25 case, various controls of the sound recording section  
and the reproduction section including the reproduction  
memory and the sound recording memory may be effected in  
bidirectional fashion. Specifically, the present



1 invention may be embodied in various modifications  
without departing from the spirit thereof.

[Effect of the Invention]

According to the present invention, the sound  
5 recording section and the reproduction section are  
separated from each other, a plurality of audio files  
extracted as desired are transferred to the reproduction  
section as index addresses, and the index addresses are  
converted into successive audio files of the reproduc-  
10 tion memory thereby to save the capacity of the repro-  
duction memory. Also, the large power for transfer and  
sound recording is supplied to the reproduction section  
from the sound recording section separated. As a  
result, the reproduction section operates at low  
15 frequency for reproduction, and reduced in internal  
power, thereby lengthening the life thereof. Further,  
an optimum memory capacity due to the content index  
system and elimination of the sound recording section,  
etc. realizes a card small in size and weight. There-  
20 fore, the portability is attained, with increased  
freedom of reproduction in terms of place and time,  
thereby expanding the range of application of audio  
digital recording. The present invention may be  
developed, for example, as a guide to various facili-  
25 ties, for introduction to commodities or handling of  
devices on display, etc.

Also, in the configuration of the reproduction  
section with a DRAM chip shown in the embodiments of the

1 present invention, the refresh counter in the reproduc-  
tion section is controlled from the sound recording  
section at the time of transfer and writing. As a  
result, coordination between memory access and refresh-  
5 ing is easy. Since the audio file can be silenced by a  
sound presence/absence flag or a file flag, on the other  
hand, a defective bit can be masked by controlling the  
audio information in blocks in a free format conforming  
to the variable-length audio file or with the word or  
10 bit line of the memory chip as a basic unit. It is  
therefore possible to use a quality memory from the  
parts which have so far been wasted. As a result, a  
DRAM low in unit bit cost and a semiconductor memory  
thus far disposed of as defective can be used, giving  
15 rise to the possibility of reducing the cost of the  
reproduction section. Also, the sound recording memory  
used with a similar semiconductor memory can be reduced  
in cost by adding a flag.

Further, the transfer of audio information  
20 from the sound recording section to the reproduction  
section is high in speed because of digital signals are  
used between memories. Also, the reproduction section,  
which is configured of a semiconductor memory, has less  
parts subjected to mechanical wear unlike in the conven-  
25 tional tape recorder or the like, and contributes to an  
improved system reliability for use under an adverse  
environment or in a place exposed to much dust or sharp  
vibrations.

1 4. Brief Description of Drawings

Fig. 1 is a block diagram showing the principle of a recording and reproduction system according to the present invention.

5 Fig. 2 is a block diagram for explaining a recording and reproduction system according to the prior art.

Fig. 3 is a block diagram for explaining a second embodiment of the present invention.

10 Fig. 4 is a block diagram for explaining a third embodiment of the present invention.

Fig. 5 is a block diagram for explaining a fourth embodiment of the present invention.

15 Fig. 6 is a block diagram for explaining a fifth embodiment of the present invention.

Fig. 7 is a block diagram for explaining a sixth embodiment of the present invention.

Fig. 8 is a block diagram for explaining a seventh embodiment of the present invention.

20 Fig. 9 is a block diagram for explaining an eighth embodiment of the present invention.

Fig. 10 shows an operation flow for explaining Fig. 9.

25 Fig. 10-1 shows the contents of a register table such as an index register, a head address register and a sound presence/absence flag for explaining Fig. 9.

Fig. 11 shows an embodiment of the contents of a register table such as an index register, a head

1 address register and a file flag for managing the audio  
information by blocks.

Figs. 12, 12-1 and 12-2 show an embodiment of  
the housings of the sound recording section and the  
5 reproduction section specifically.

#### Designation of Reference Numerals

2, 2' ... Sound recording section; 4 ...  
Reproduction section, 6 ... Input signal; 8 ... A/D  
conversion section; 10 ... Sound recording memory;  
12 ... Sound recording control section; 14 ... Sound  
recording display section; 16 ... Sound recording  
operating section; 16' ... Operating section for sound  
recording and reproduction; 28, 28' ... Output signal;  
18 ... D/A conversion section; 20 ... Reproduction  
memory; 22 ... Reproduction control section; 24 ...  
Reproduction display section; 26 ... Reproduction  
operating section; 30 ... Digital signal; 32 ... Control  
signal for the reproduction control section 22 and index  
address signal for the reproduction memory 20; 34 ...  
Standby control signal; 52 ... Sound recording control  
signal; 54, 54' ... Reproduction control signal; 130a,  
132a, 134a ... Connection terminal group for sound  
recording section 2; 130b, 132b, 134b ... Connection  
terminal group for reproduction section; 42 ... Sound  
recording display control signal; 44 ... Operating  
signal for sound recording control section; 48 ...  
Reproduction display control signal; 50 ... Operating

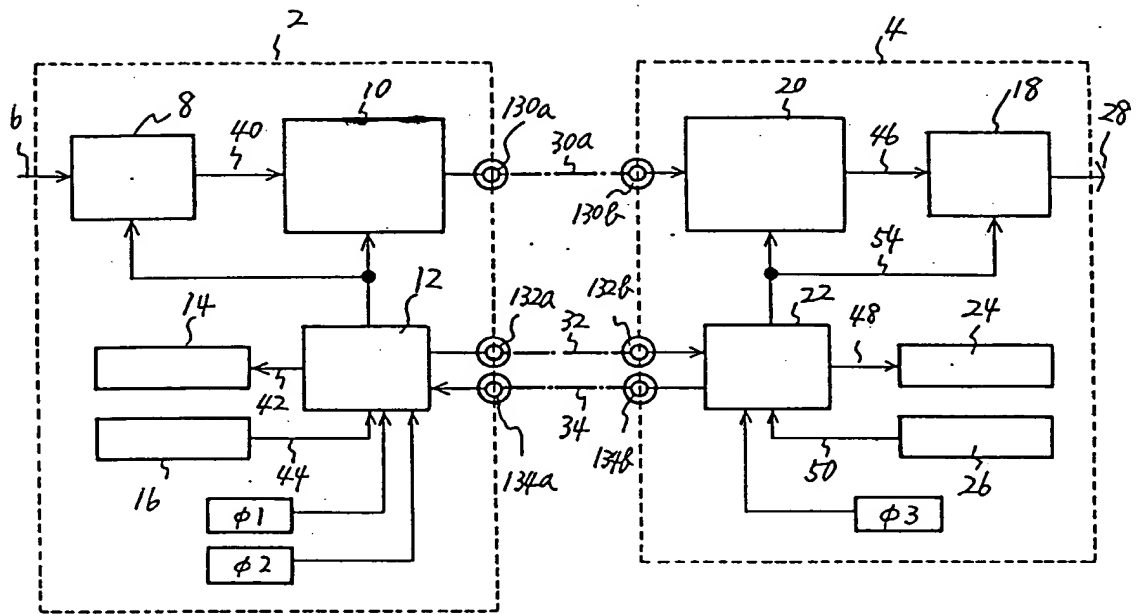
signal for reproduction control section; Mr ... Memory capacity of sound recording memory 10; Ms ... Memory capacity of reproduction memory 20; 8a ... Input amplifier; 8b ... Low-pass filter; 8c ... A/D conversion circuit; 56 ... Recognition (identification) circuit of reproduction section 4; 58 ... Power circuit of sound recording section 2; 60 ... Power circuit of reproduction section 4; 64 ... I/O slot; 18a, 18a' ... D/A converter; 18b, 18b' ... Low-pass filter; 18c, 18c' ... Output amplifier; 62 ... Change-over switch; 70 ... Optical disk; 72 ... buffer memory; 74 ... Transmission circuit; 76 ... Transmitting antenna; 78 ... Receiving antenna; 80 ... Receiving circuit; 90 ... Wireless receiver; 100 ... Externally written semiconductor memory; 100' ... Externally written optical disk, magnetic disk and digital audio tape; 12a ... Control circuit of sound recording control section 12; 12b ... Index address register; 12c ... Address counter; 22a ... Control circuit of reproduction control section 22; 22b, 22b' ... Register table; 22c ... Address counter; 110 ... Clear circuit; 112 ... Clear energization signal; 32a ... Index address signal; 32b ... Control signal for reproduction control section 22a; 32c ... DRAM refresh demand signal; 34 ... Ready signal; 52a ... Address signal for sound recording memory 10; 52b ... Memory control signal for sound recording memory 10; 52c ... Activation signal for A/D conversion circuit 8c; 54a ... Address signal for reproduction memory 10; 54b ...

Memory control signal for reproduction memory 10;  
54b ... Activation signal for D/A conversion circuit  
18c; 114 ... Index address setting signal; 116 ...  
Counter activation signal; 118 ... Signal for setting  
index address; 120 ... Counter activation signal;  
122 ... Address counter output feedback signal; 138,  
140, 140' ... Index address register for reproduction  
control section; 142, 142' ... Head address register;  
144 ... Sound presence/absence flag bit; 146 ... File  
flag bit; 200 ... Small-size storage processing device  
such as memory card or IC card; 210 ... Speaker.

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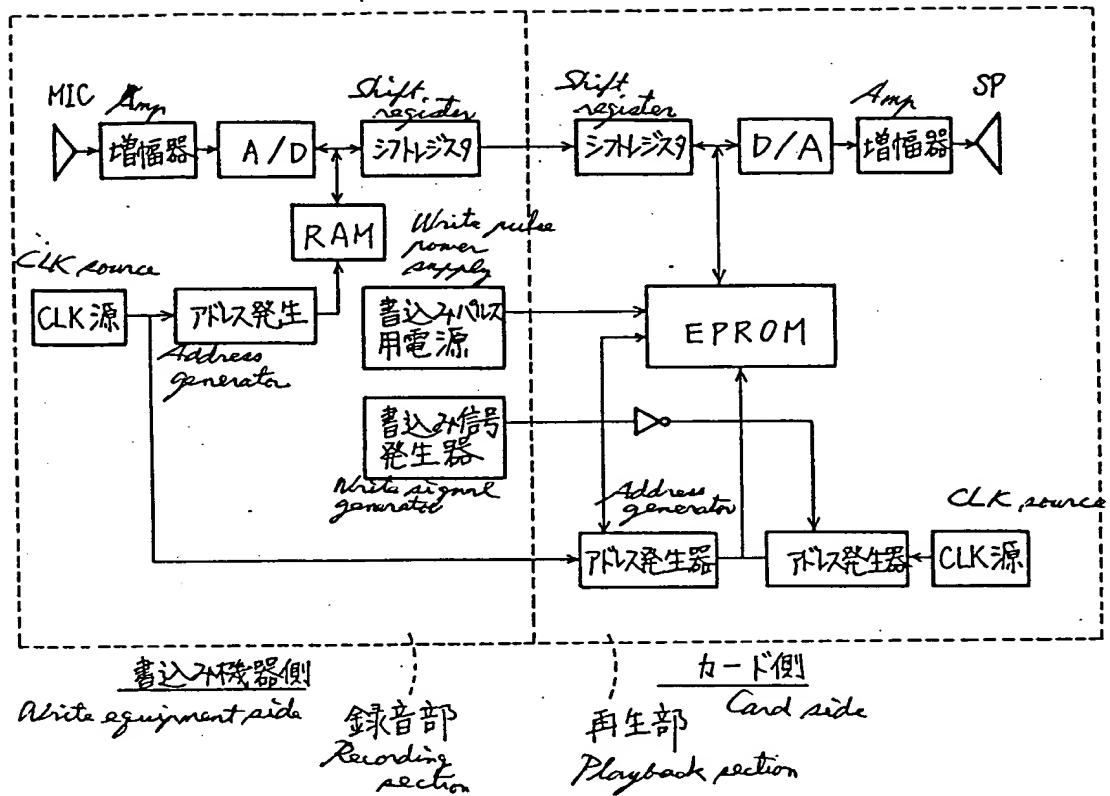
第1図 Fig. 1



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第2図 Fig. 2



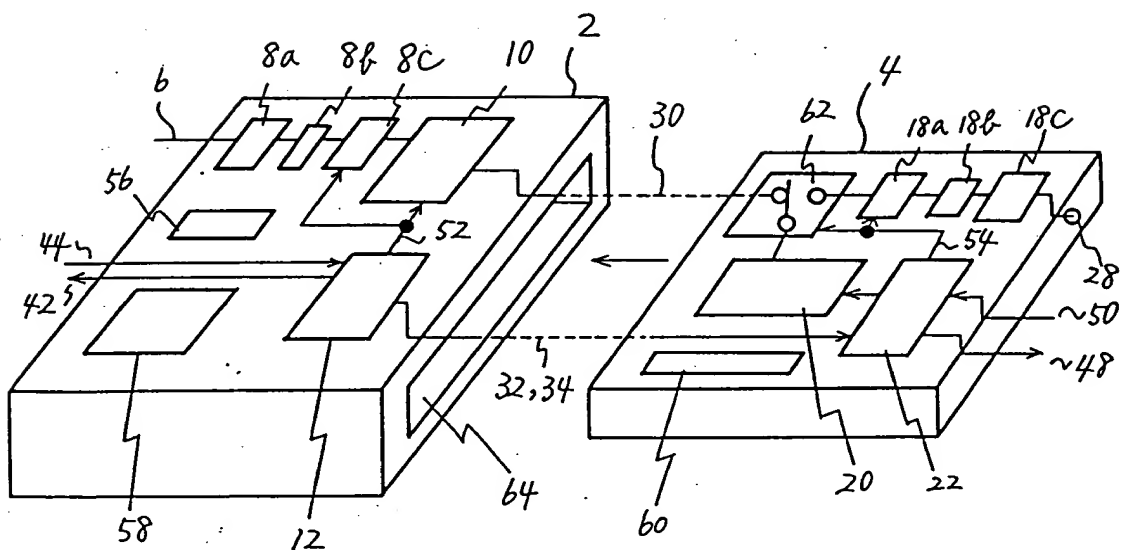
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第3図

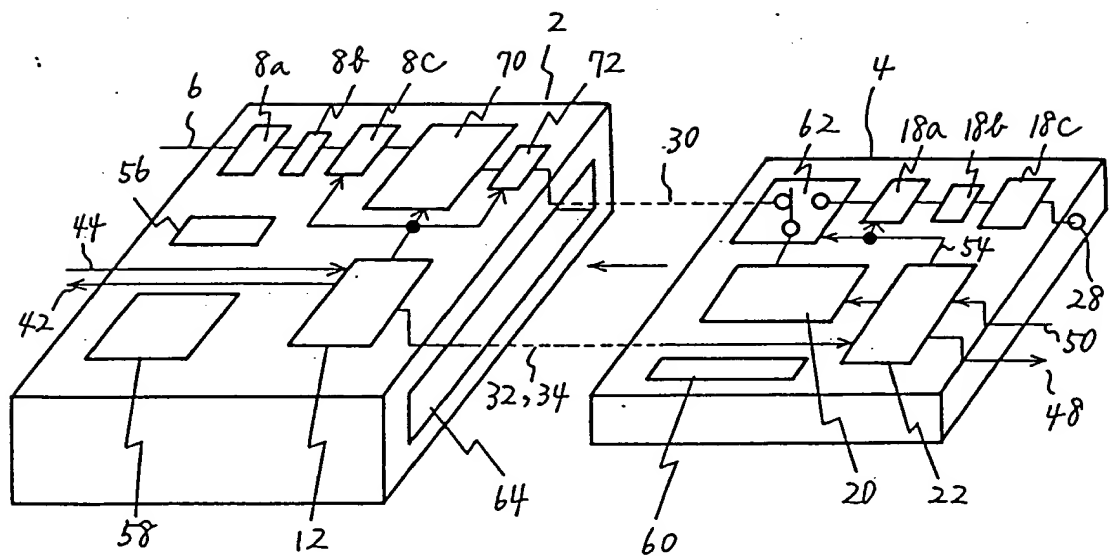
Fig. 3



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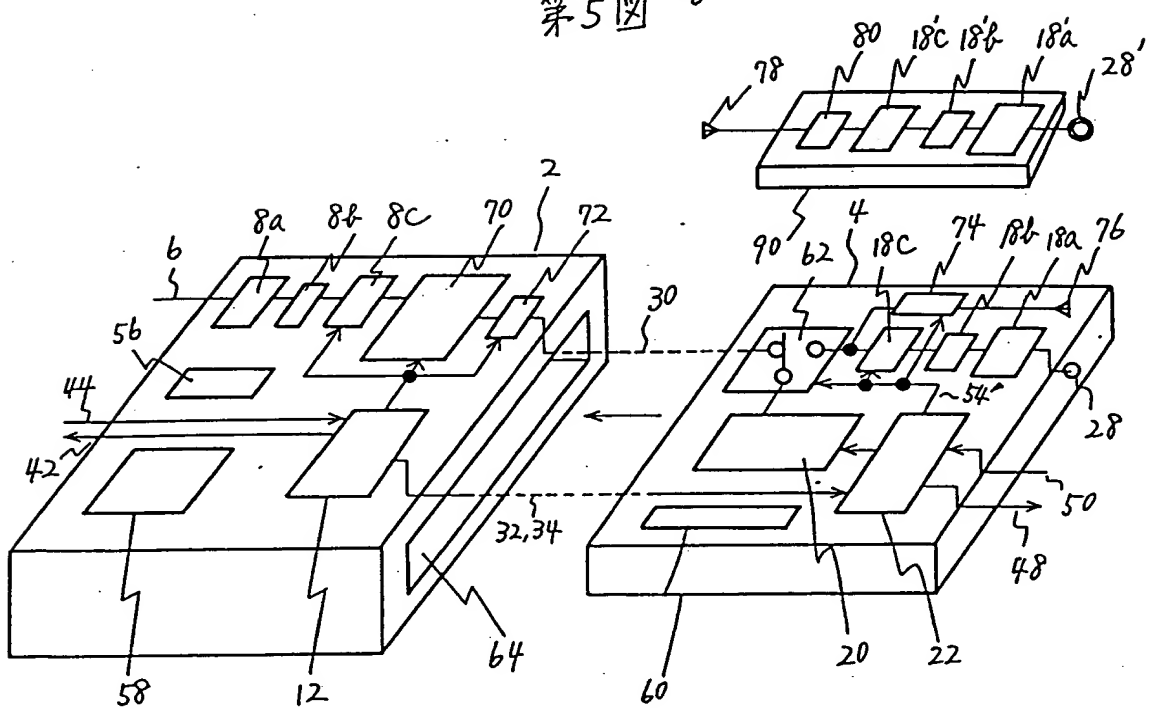
第4図 Fig. 4



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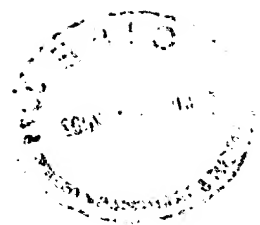
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第5圖 Fig. 5

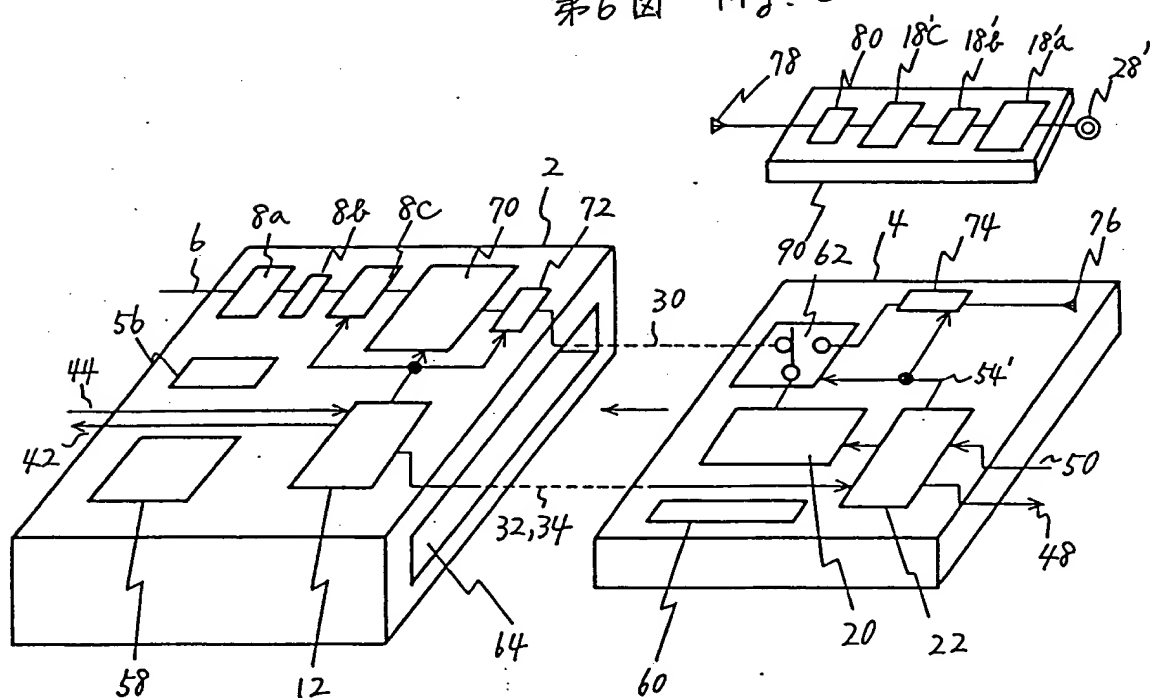


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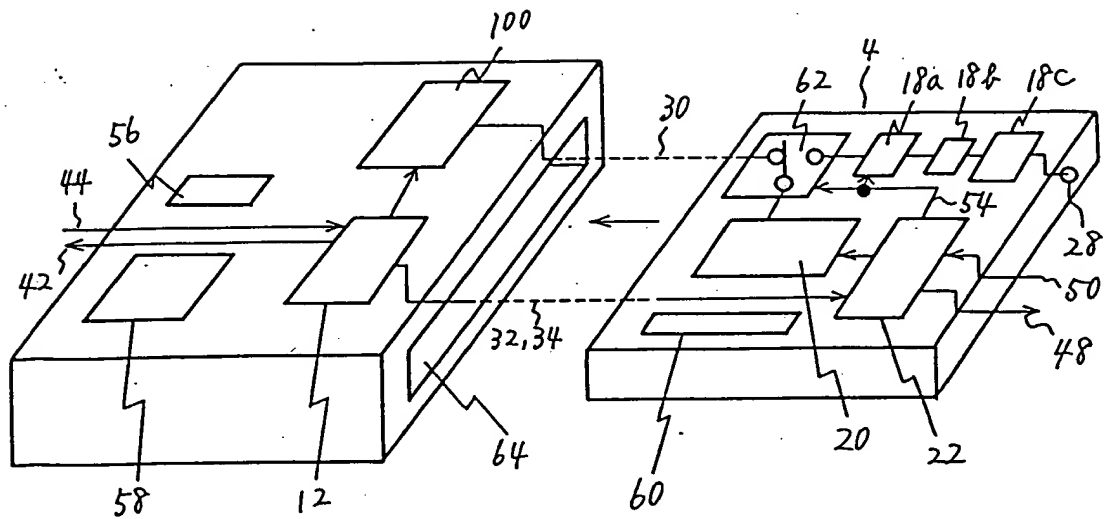


第6図 Fig. 6

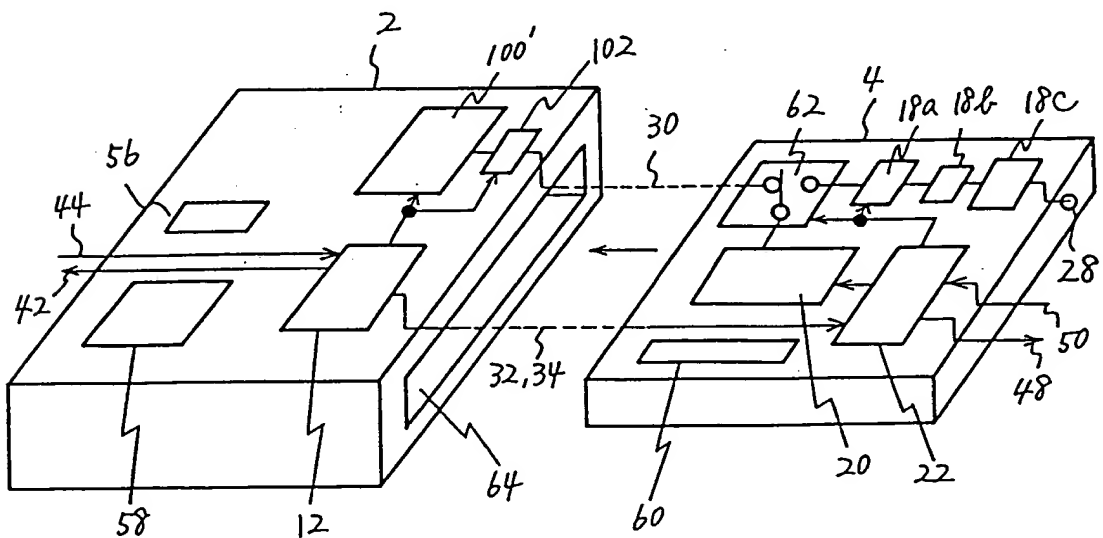


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第7図 Fig. 7



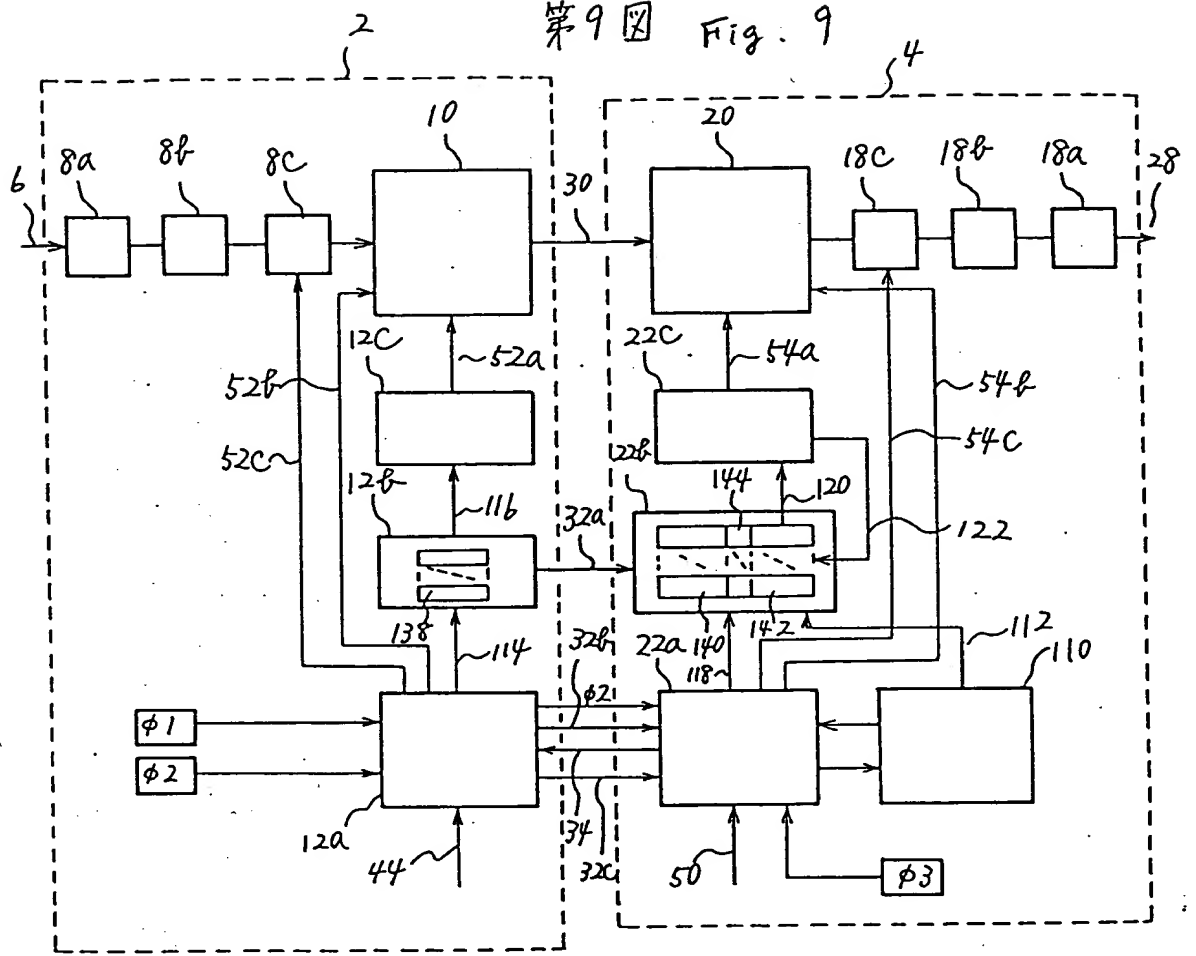
第8図 Fig. 8



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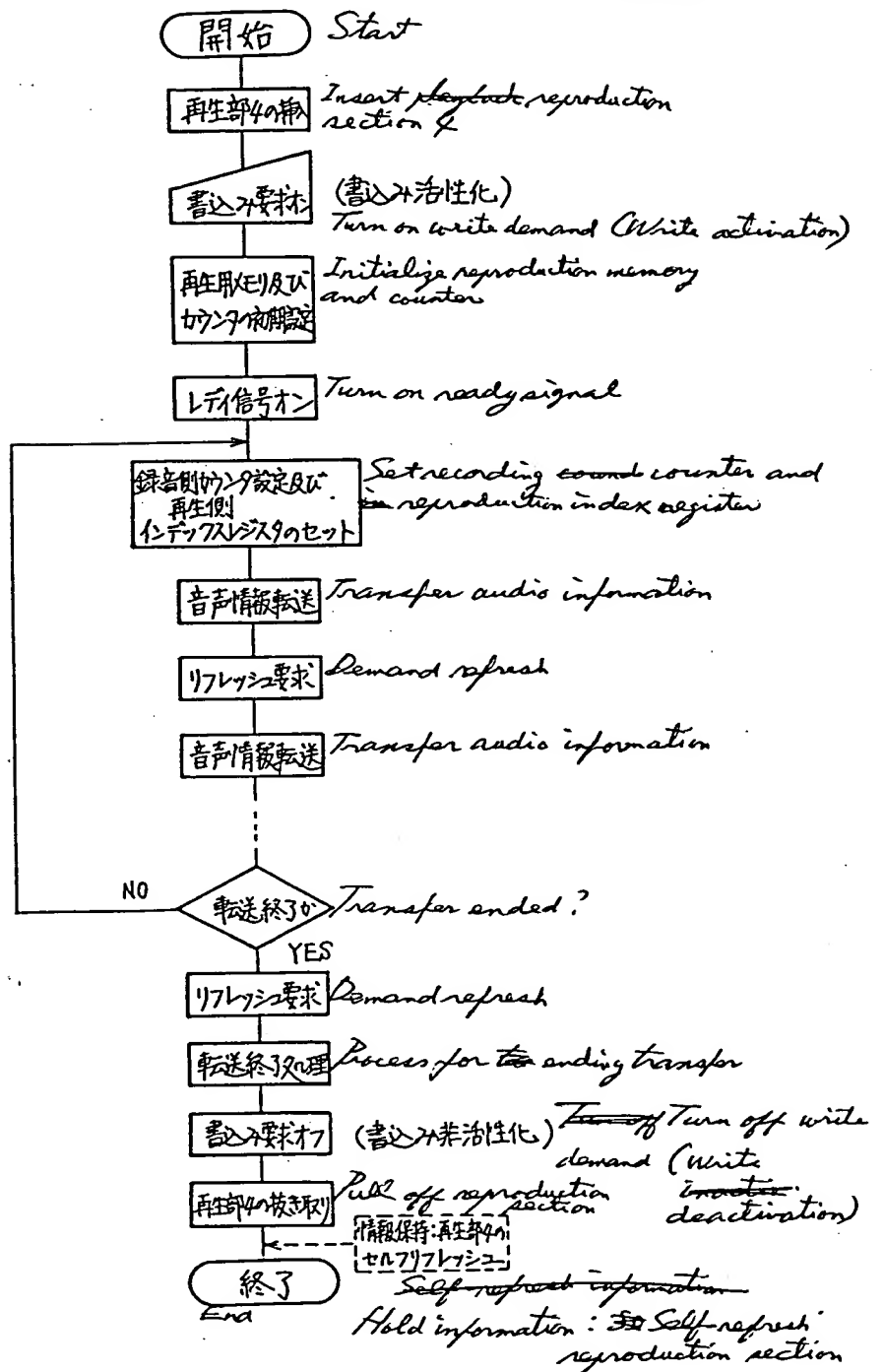


第9図 Fig. 9



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第10図 Fig



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Fig. 10 - 1

Index address register  
(36 bit)

第10-1図

Head address  
register  
(32 bit)

Sound  
presence/  
absence  
flag

例 Ex.	インデックスアドレスレジスタ (36ビット)	例	インデックスアドレスレジスタ (36ビット)	先頭アドレスレジスタ (32ビット)	音声無 マク
(1)	000---000000000	(s1)	000---000000011	00---00000000	1
(2)	000---000000011	(s2)	000---000001100	00---00001001	1
(3)	000---000001100	(s3)	000---000100001	00---00010001	1
(4)	000---000010100	(s4)	000---011010110	00---00100011	1
(5)	000---000100001	(s5)	111---111111111	00---00111000	0
(6)	000---001010111				
(7)	000---011010110				
(8)	000---011101011				
⋮	⋮				
(n)	101---111110001				
(n+1)	111---110000011				

(音声ファイルの終了指示)  
アドレス

(End designation address)  
for audio file

(音声ファイルの最終アドレス  
+1の値)

(Final address of  
audio file + 1)

(最終の音声ファイルの初期値)

(Initial value of ~~last~~  
audio file)

(録音部の最終アドレス値)

(~~last~~ Final address value)  
of recording section

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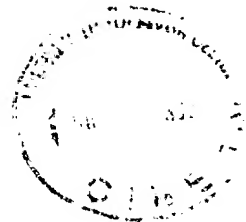
Index address register (14 bits) 140  
Head address register (10 bits) 142  
File flag 146  
Fig. 11  
第11図  
Remark

例 Ex.	インデックスアドレスレジスタ (14ビット)	先頭アドレスレジスタ (10ビット)	ファイルフラグ		備考
(1)	00001001100001	0000000000	0	1	音声ファイルの開始
(2)	XXXXXXXXXXXXXXXX	0000000001	1	0	" 1の続き
(3)	XXXXXXXXXXXXXXXX	0000000010	1	0	" 1の続き
(4)	XXXXXXXXXXXXXXXX	0000000011	1	1	" 1の終了
(5)	01010101111000	0000000100	0	1	" 2の開始
(6)	XXXXXXXXXXXXXXXX	0000000101	1	1	" 2の終了
⋮	⋮	⋮	⋮	⋮	⋮
(n-9)	10000001110001	1111110110	0	1	音声ファイルの開始
⋮	⋮	⋮	⋮	⋮	⋮
(n-6)	XXXXXXXXXXXXXXXX	1111111001	1	1	音声ファイルの終了
(n-5)	11111111111111	1111111010	0	0	音声ファイルなし
(n-4)	XXXXXXXXXXXXXXXX	1111111010	0	0	音声ファイルなし
⋮	⋮	⋮	⋮	⋮	⋮
(n)	XXXXXXXXXXXXXXXX	1111111010	0	0	音声ファイルなし

(記号:Xは内容不明、"0","1"レベル不明可)

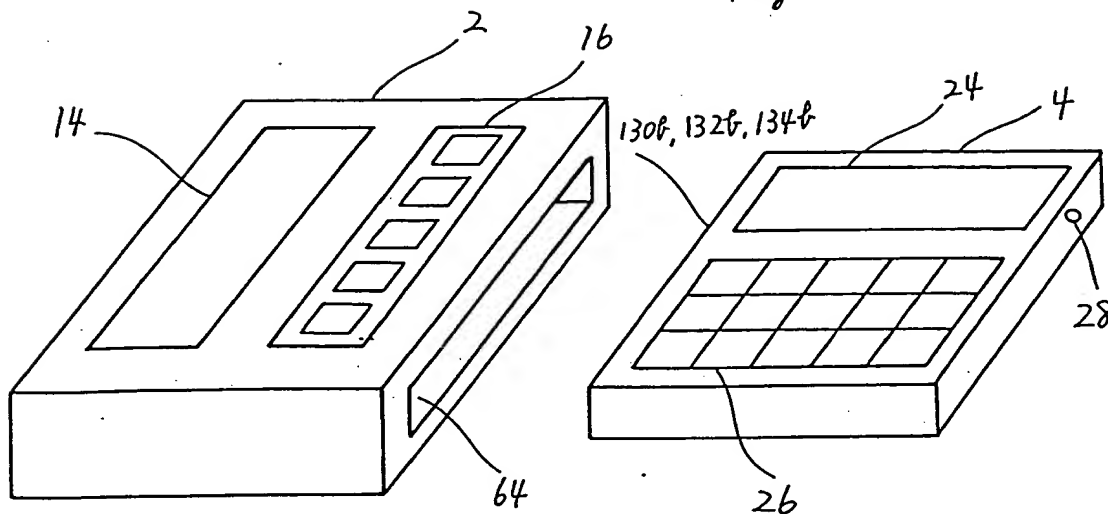
(Symbol: X indicates "Don't care" and may be "0" or "1")

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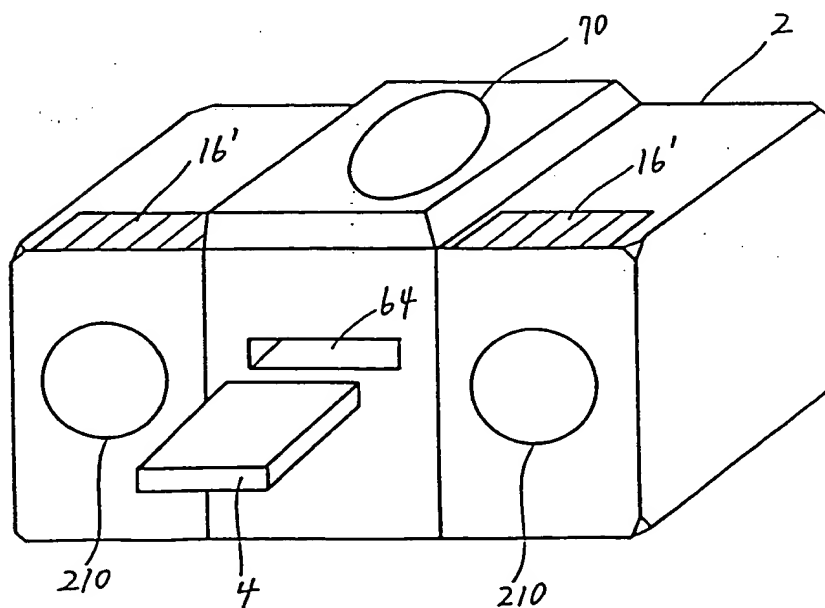


第12図

Fig. 12



第12-2図 Fig. 12-2



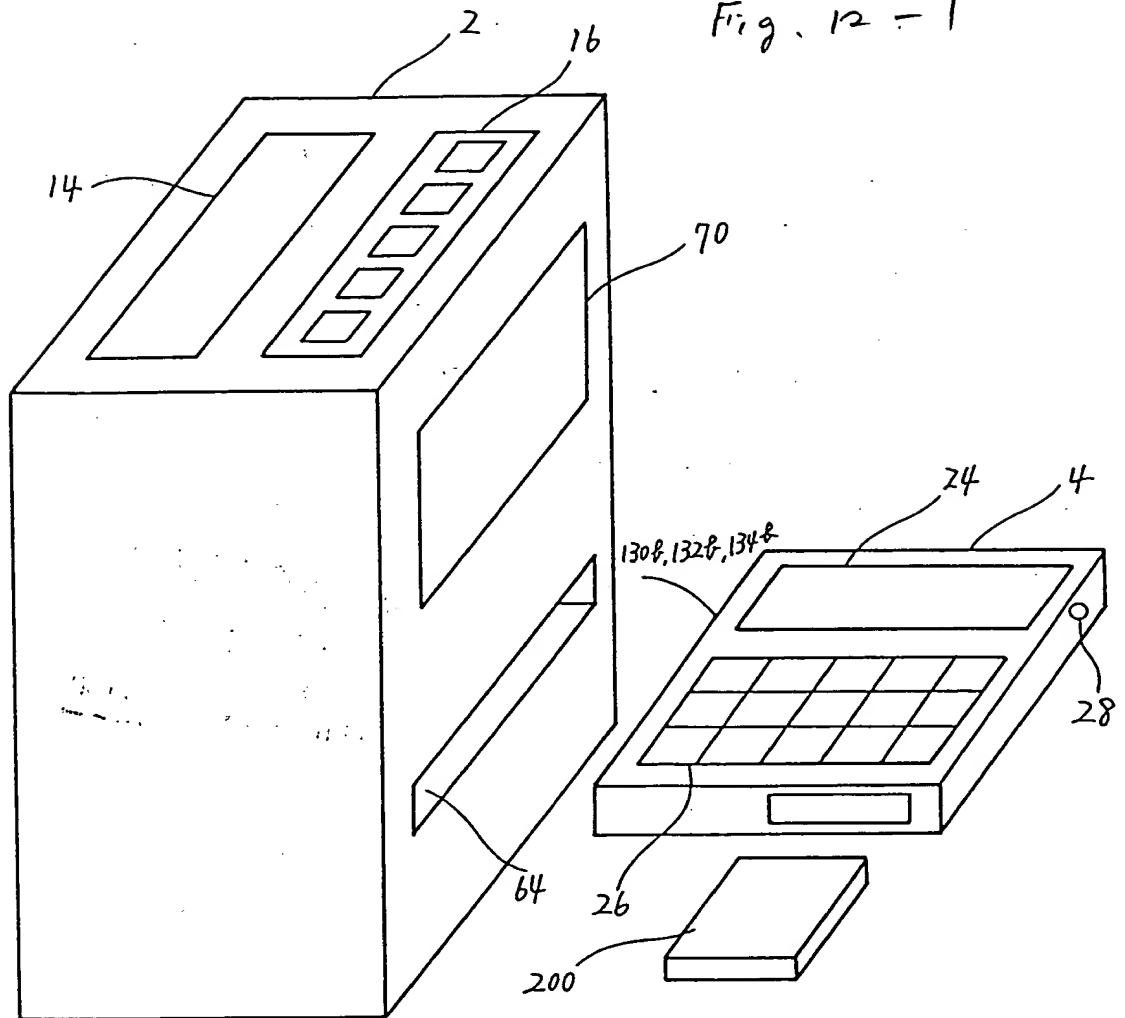
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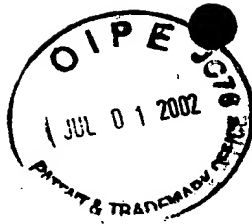
第12-1圖

Fig. 12-1



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DECLARATION

I, Michiyuki MORITA , a national of Japan, c/o Asamura Patent Office of 331-340, New Ohtemachi Building, 2-1, Ohtemachi-2-chome, Chiyoda-ku, Tokyo, Japan do hereby solemnly and sincerely declare:-

- 1) THAT I am well acquainted with the Japanese language and English language, and
- 2) THAT the attached is a full, true and faithful translation into the English language made by me of Japanese Patent Application No. 3-57972

The undersigned declares further that all statements made herein of his own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001, of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Signed this 31st day of January , 1994.

*Michiyuki Morita*

Michiyuki MORITA

[Title of Document] Patent Application

[Reference Number] H1002521

[Date of Submission] February 27, 1991

[Addressee] The Director-General  
The Patent Office

[International Patent Classification] G11C 11/34

[Title of the Invention] DIGITAL SIGNAL RECEIVING/  
DELIVERY SYSTEM, DIGITAL  
AUDIO SIGNAL PROCESSOR AND  
SIGNAL CONVERTER

[Number of Claim(s) for a Patent] 29

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[Title of Article]	Specification -----	1
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1 [Title of Document] Specification

[Title of the Invention] DIGITAL SIGNAL RECEIVING/  
DELIVERY SYSTEM, DIGITAL  
AUDIO SIGNAL PROCESSOR AND  
5 SIGNAL CONVERTER

[Scope of Claim for a Patent]

[Claim 1] A digital signal receiving/delivery  
system characterized by comprising a digital signal  
source, and a player electrically connected substan-  
10 tially one-to-one to the digital signal source,  
receiving and storing a specified digital signal in a  
memory in the form of electrical signal and reproducing  
a digital signal independently stored.

[Claim 2] A digital signal receiving/delivery  
15 system according to Claim 1, characterized in that the  
digital signal source includes a digital signal supply,  
and a terminal unit for receiving and storing a digital  
signal from the signal supply through a communication  
channel or an appropriate storage medium as required  
20 and receiving/delivering a specified digital signal,  
said digital signal supply being electrically connected  
with the player in one-to-one relationship through a  
connector.

[Claim 3] A digital signal receiving/delivery  
25 system according to Claim 2, characterized in that the

1 terminal unit uses a magnetic disk memory unit having a  
comparatively large storage capacity as a backup memory,  
and a digital signal received/delivered in great amount  
with the player or a digital signal updated with the  
5 lapse of time is stored in a buffer memory configured of  
a semiconductor memory accessible with high speed.

[Claim 4] A digital signal receiving/delivery  
system according to Claim 2 or 3, characterized in that  
the terminal unit has the function of a microcomputer,  
10 manages the magnetic disk memory and the buffer memory,  
exchanges a digital signal with the signal supply  
through a communication channel, and also manages a  
storage area of a memory in the player connected.

[Claim 5] A digital signal receiving/delivery  
15 system according to Claim 2, 3 or 4, characterized in  
that the terminal unit has the function of reproducing  
and outputting a part of a designated digital signal for  
a predetermined time.

[Claim 6] A digital signal receiving/delivery  
20 system according to Claim 2, 3, 4 or 5, characterized in  
that the player has a secondary battery built therein,  
and when connected with the terminal unit, charges the  
secondary battery from the power supply on the terminal  
unit side.

25 [Claim 7] A digital signal receiving/delivery  
system according to Claim 1, 2, 3, 4 or 6, characterized  
in that the digital signal is a digital audio signal,  
and the player has a reproduction output circuit for



1 outputting by converting a digital audio signal read  
from the memory into an analog audio signal.

[Claim 8] A digital signal receiving/delivery  
system accordnig to Claim 1, 6 or 7, characterized in  
5 that the memory is made in the form of a thin card  
storage medium and mountable/demountable against the  
player.

[Claim 9] A digital signal receiving/delivery  
system according to Claim 1, 2, 3, 4, 6, 7 or 8,  
10 characterized in that the digital signal received/  
delivered as above has an ID code, and the condition for  
reproduction in the player is automatically designated  
in accordance with the contents of the ID code.

[Claim 10] A digital signal receiving/delivery  
15 system according to Claim 9, characterized in that the  
condition for reproduction includes at least one of  
stereo/monaural, a resolution of 8 or 6 bits and a  
sampling frequency.

[Claim 11] A digital signal receiving/delivery  
20 system according to Claim 6, 7 or 8, characterized in  
that the player has an outline and a connector  
compatible with the existing memory.

[Claim 12] A digital signal receiving/delivery  
system according to Claim 6, 7, 8 or 11, characterized  
25 in that the memory of the memory section has the  
function usable equivalently to the existing memory  
card.

1        [Claim 13] A digital signal receiving/delivery  
system according to Claim 1, 6, 7, 8, 9, 10, 11 or 12,  
characterized in that the player has a security function  
for reversing at least one-bit digital signal of the  
5 input and/or output section of the memory or replacing  
with other bits in accordance with a password or a  
password coincidence detection signal.

      [Claim 14] A digital signal receiving/delivery  
system according to Claim 1, 6, 7, 8, 9, 10, 11 or 12,  
10 characterized in that the player has the security  
function of reversing at least one-bit digital signal at  
the address input section of the memory or replacing  
with another bit in accordance with a password or a  
password coincidence detection signal.

15        [Claim 15] A digital signal receiving/delivery  
system according to Claim 1, 6, 7, 8, 9, 10, 11, 12, 13  
or 14, characterized in that the player includes a  
storage area or a content memory for storing content  
information including a storage address corresponding to  
20 a plurality of digital signals, and a data area or a  
data memory accessed by the storage address.

      [Claim 16] A digital signal receiving/delivery  
system according to Claim 1, 6, 7, 8, 9, 10, 11, 12, 13,  
14 or 15, characterized in that the player has a  
25 plurality of types of operating modes designated by the  
turn-on time or the number of turnings on of a single  
key switch.

1        [Claim 17] A digital audio signal processor  
characterized in that a voice interval of a digitized  
audio signal is detected, and a digital signal inputted  
to a digital/analog converter during the particular  
5 voice interval is forcibly replaced with a signal  
corresponding to the AC zero level.

      [Claim 18] A digital audio signal processor  
according to Claim 17, characterized in that the voice  
interval is detected on condition that the voice  
10 interval continues for a predetermined time, on the  
basis of output signals of a pair of comparators for  
comparing the magnitude between a reproduced digital  
signal and a digital signal corresponding to a level  
considered silent of adjustable positive and negative  
15 electrodes respectively.

      [Claim 19] A digital audio signal processor  
characterized in that a voice interval of a digitized  
audio signal is detected and is enlarged for slow  
playback.

20        [Claim 20] A digital signal processor according to  
Claim 19, characterized in that the means for enlarging  
the voice interval functions by substantially delaying  
the address-updating operation of the memory circuit  
storing a digital signal as compared with normal  
25 operation.

      [Claim 21] A digital audio signal processor  
characterized in that a voice interval of a digitized

1 audio signal is detected, and the particular voice  
interval is shortened to perform fast playback.

[Claim 22] A digital signal processor according to  
Claim 21, characterized in that the means for shortening  
5 the voice interval increases the address-updating speed  
of the memory circuit storing a digital signal as  
compared with the normal operation.

[Claim 23] A digital signal processor charact-  
erized in that a voice interval of a digital signal is  
10 replaced by voice interval code information and voice  
interval time information for data compression, the  
address-updating operation of a memory is stopped and a  
signal corresponding to an AC-like zero level is out-  
putted in its place over a time length corresponding to  
15 the voice interval time information upon detection of  
the voice interval code information under normal  
operation, the address-updating operation of a memory is  
stopped and a signal corresponding to the AC-like zero  
level is outputted in its place over a time length  
20 enlarged against the voice interval time information  
upon detection of the voice interval code information  
under the slow playback operation, and a digital signal  
is outputted ignoring the voice interval code informa-  
tion and the voice interval time information substan-  
25 tially under the fast playback operation.

[Claim 24] A digital signal processor according to  
Claim 23, characterized in that the voice interval code  
information is configured of a combination of at least

1 successive digital signals corresponding to a substan-  
tially positive maximum value and a substantially  
negative maximum value.

[Claim 25] A digital signal processor accordnig to  
5 Claim 19, 20 or 23, characterized by comprising the  
function of setting a maximum voice interval, and  
limiting the voice interval enlarged with the slow  
playback operation not to exceed the maximum voice  
interval time.

10 [Claim 26] A signal converter comprising a memory  
for receiving a digital input signal, a counter for  
receiving a reference time pulse and performing the  
counting operation correponding to the maximum value of  
a digital input signal, a comparator for comparing an  
15 output signal of the memory with an output signal of the  
counter circuit, a repeat counter for performing the  
repetitive counting operation of the counter, and a  
control circuit for designating the retrieval of an  
input digital signal to the memory in response to a  
20 strobe signal, starting the counting operation of the  
counter and transmitting a conversion-over signal from  
the output signal of the repeat counter, wherein a pulse  
width modulation signal corresponding to the digital  
input signal is obtained from the output of the  
25 comparator.

[Claim 27] A signal converter characterized by  
comprising a down-counter circuit for counting reference  
time pulses in response to a digital input signal

1 supplied at regular intervals of time corresponding to  
the maximum value of the digital signal, and a digital  
circuit for forming a pulse corresponding to the  
operating time of the down-counter circuit, wherein a  
5 pulse width modulation signal corresponding to the  
digital input signal is obtained.

[Claim 28] A signal converter according to Claim  
27, characterized in that a predetermined period  
corresponding to the maximum value of the digital signal  
10 is formed by an up-counter circuit for performing the  
counting operation corresponding to a digital input  
signal in response to the reference time pulse.

[Claim 29] A signal converter according to Claim  
26, 27 or 28, characterized in that the pulse width  
15 modulation signal is converted into an analog signal by  
being inputted to a low-pass filter including a resistor  
and a capacitor.

#### [Detailed Description of the Invention]

[0001]

20 [Industrial Field of Utilization]

The present invention relates to a digital  
signal receiving/delivery system, a digital audio signal  
processor and a signal converter, such as a digital  
signal receiving/delivery system for realizing sale or  
25 supply of specified audio data or the like by trans-  
mitting it to a specified person in the form of  
electrical signal, and a technique effectively used for

1 an audio signal processor and a signal converter  
suitable for the system.

[0002]

[Prior Art]

5 As a conventional example of commercialized  
information, there is a newspaper or magazine on which  
characters or the like are printed by use of paper as a  
medium. The paper used in this way may be replaced by  
various types of software sold through a memory medium  
10 such as floppy disk, or IC card. Another example is  
communication means such as cable television or satel-  
lite broadcasting for supplying news or broadcast  
programs to specified subscribers.

Further, a portable computer, which unlike the  
15 conventional notebook-type personal computer or "elec-  
tronic notebook", can easily send a message to another  
person, access a data base, or process information  
without being restricted by time or place, has been  
suggested in "Nikkei Electronics", November 26, 1990,  
20 pp.116 to 124. This system proposes data transmission  
to a portable terminal through public telephone or FM  
broadcasting or sale of IC cards at bookstores or  
station booths.

Further, JP-A-61-236222 suggests a digital-to-  
25 analog converter that can be realized by a digital  
circuit.

1

[0003]

[Problem that the Invention is to Solve]

In the case where information is commercial-  
ized and sold by use of paper as a medium as in news-  
5 papers or magazines, the printing and transportation  
take long time, which not only makes the system un-  
suitable for timely sale of information, but also  
adversely affects the earth environment by deforestation  
for making paper and discharging information garbage.  
10 In the case where a IC card or floppy disk is used as a  
medium as in the electronic notebook or the like, a  
terminal device such as the electronic notebook or  
personal computer is needed. In addition, these  
terminal devices presuppose information processing such  
15 as in the electronic notebook, so that the operation  
thereof is comparatively complicated and difficult in  
application, thereby preventing general extension of the  
use thereof. Also, in the case where a great amount of  
data are distributed through FM broadcasting, it is  
20 troublesome to select necessary information, and as in  
the case of the satellite or cable television broad-  
casting, even unnecessary information is received under  
a blanket contract.

[0004]

25

Accordingly, the present inventors have  
developed a digital signal receiving/delivery system  
which makes it possible to deliver and receive informa-  
tion in the same form as general commodities as an



1 electrical signal, and a digital audio signal processor  
and a signal converter suitably used therewith.

An object of the present invention is to  
provide a digital signal receiving/delivery system  
5 realizing the sale of information or the like having a  
commercial value in the form of electrical digital  
signal.

Another object of the present invention is to  
provide a digital audio signal processor realizing a  
10 variety of forms of reproduction of high quality of  
digital audio signal.

A still further object of the present  
invention is to provide a signal converter suitable for  
a digital circuit used for digital/analog conversion or  
15 the like.

The foregoing and other objects and novel  
features of the present invention will become apparent  
from the description of this specification and the  
accompanying drawings.

20 [0005]

[Means for Solving the Problem]

A typical example of the systems according to  
the present invention disclosed by the present patent  
application will be briefly described. In the process  
25 of receiving of a digital signal, a player is elec-  
trically connected as a terminal device to a digital  
signal source in one-to-one correspondence, so that a  
specified digital signal is received and stored in a

1 memory in the form of electrical signal, and then the  
stored digital signal can be independently reproduced in  
the player. The voice interval of a digitized audio  
signal is detected. This voice interval is enlarged to  
5 realize slow playback, and is shortened to attain fast  
playback. A signal of a pulse width corresponding to  
the digital input signal is repeated a plurality of  
times during a single signal conversion period.

[0006]

10 [Operation]

The player receives a digital signal in the  
form of electrical signal, and independently play backs,  
so that the value of the digital signal received can be  
exhibited in direct form. As a consequence of the  
15 usability of a digital signal in direct form, a system  
for processing, production and sale thereof is con-  
figured easily. At the same time, the simple player  
construction offers the handling ease for every user.  
By enlarging or extending the voice interval of a  
20 digital audio signal substantially, fast or slow play-  
back is made possible without deteriorating the sound  
quality. And, by forming a repetitive pulse width  
modulation signal corresponding to the digital input  
signal, the ripple associated with smoothing can be  
25 greatly reduced, thereby producing a high-quality analog  
signal.

1

[0007]

[Embodiments]

5

A block diagram of the essential parts of a digital signal receiving/delivery system according to an embodiment of the present invention is shown in Fig. 1. This embodiment is intended for a system to commercialize and sell a digital signal. In other words, the sale of the information is made available as one of forms of receiving and delivery of a digital signal.

10

15

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25

In Fig. 1 is shown a block diagram of a terminal device of all the digital signal selling systems. This terminal device is equivalent to a vending machine for cigarettes or soft drinks such as juice and functions as an information server. The terminal equipment, though not specifically limited, is connected to an original supplier of a digital signal through a broad band integrated services digital network (B-ISDN) to receive the digital signal as a commodity without specific limitation. As a result of employment of this system, the digital signal is transferred only to a specified terminal device through a communication network in a manner similar to such commodities as cigarettes and juice. In this case, the digital signal as a commodity can be transferred at high speed and in a great amount, free of any traffic jam or air pollution unlike in the case of general commodities. The terminal device is installed in front of a store like a station booth, a cigar stand or a book shop.

1           The terminal device is roughly comprised of an  
input section, a memory section and an output section.  
Each circuit block, which is connected by a VME bus, is  
adapted to receive digital and various control signals.  
5   This terminal device, which is connected to a player  
shown by dotted line in Fig. 1, is used to directly  
receive a specific digital signal as a commodity.

[0008]

Fig. 2 is a block diagram showing an input  
10   section of the terminal device. The input section of  
the terminal device has a digital input interface INF  
for the broad band integrated services digital network  
(B-ISDN) and an analog input interface (right and left  
analog inputs) for receiving an input signal in an  
15   analog form. The analog input interfaces are provided  
with low-pass filters LPF, associated with the right  
input Rin and the left input Lin, for eliminating  
extraneous frequency band components contained in the  
analog input signals Rin and Lin in advance, respec-  
20   tively. These input signals Rin and Lin are alternately  
selected through a multiplexer MPX with respect to time,  
introduced to a sample-and-hold circuit S/H and  
converted into a digital signal by an analog-to-digital  
converter ADC. At this time, the analog-to-digital  
25   converter ADC outputs two-channel (stereo) time-shared  
digital signals of right and left channels in time  
series, which signals are introduced to the digital  
input interface INF. Such analog input interfaces are

1 used for digitalizing and storing music programs,  
regular news, stock market information, various  
commodity market situations or the like sent by  
broadcasting in a memory.

5 A monaural signal is inputted as the above-  
mentioned right or left input signal. The function may  
be added to broaden band widths of the low-pass filters  
LPF for input signals having a broad band widths such as  
music, and to narrow the band widths of the low-pass  
10 filters LPF for input signals having narrow band widths  
such as news. INCT designates an input section  
controller, and NIF shown by dotted line a network  
interface corresponding to the B-ISDN.

[0009]

15 Each analog input interface may be adapted to  
receive a message from an automatic answering telephone  
set by being connected to a telephone line. In such a  
case, the function of a telephone set may be added to  
the terminal device connected with the automatic answer-  
20 ing telephone set to receive a recorded message there-  
from. When the analog input interface is used in this  
way, the message transfer time is undesirably lengthen-  
ed. If a subscriber to a digital line system uses a  
digital automatic answering telephone set to store mes-  
25 sages in a digital form, the messages recorded can be  
received in a very short time, and by doing so, the user  
can confirm the messages, at the desired time while be-  
ing in transportation means or under the like situation.

1 [0010]

Fig. 3 is a block diagram showing an embodiment of the memory section in the terminal device. This memory section includes an external memory like a hard  
5 disk memory HDD, a RAM (random access memory) as a buffer memory, a ROM (read only memory) for storing various programs, and a microprocessor CPU for processing information or performing control operations in accordance with these programs. The programs include  
10 the information-processing program for a digital or analog input operation, a data exchange operation with the hard disk memory HDD, a display operation of a liquid crystal display LCD or a data transfer operation with a player connected to the output section. The RAM,  
15 though not specifically limited in capacity, has a storage capacity of approximately 1 MB, and the ROM a storage capacity of approximately 512 KB (kilobyte as referred to in the same way hereinafter). The hard disk memory HDD, though not specifically limited in capacity,  
20 has a storage capacity of approximately 250 MB (megabyte as referred to in the same way hereinafter), and has a function as a backup memory in case of power failure or interception. In addition, it functions like a warehouse for storing a great variety of digital signals.  
25 This hard disk memory HDD, which is connected to an internal bus through a hard disk controller HDDC, is adapted to write and read data in response to an instruction from the microprocessor CPU.

1 [0011]

The LCD is a liquid crystal display and is used for displaying information menu, operating instructions, etc. The surface of the LCD with a touch-key function is used for selecting one of the displayed menu, display switching, etc. When the player is connected, for example, (1) Music, (2) news, (3) Weather forecasting, (4) Stock market situation, (5) Reading, etc. are displayed as the first information menu on the display screen. If one of them, say, (2) News is selected, the screen is shifted to display (1) NHK, (2) FEN, (3) Traffic information, (4) Sports, etc. By designating a desired one of these news programs, a digital signal corresponding to the selected program is received by the player.

In a case of (1) Music, for instance, such music categories as classic, popular and jazz are displayed, so that if a specific music category is selected, a name of a marketable music is displayed. Such music information, though not specifically limited, is assumed to be stored in a specific area of the hard disk memory or the ROM. When the desired music is not available in the hard disk memory HDD, the device is connected to an original supplier of the digital signals through the communication channel B-ISDN to transmit an intended music program to the player. The LCD, which is connected to the internal bus through an LCD controller LCDC, is used for the above-mentioned display and input

1 operations through the touch keys.

A bus interface VMEINF is a VME bus interface for connecting the internal bus and the VME bus to each other.

5 [0012]

The news, the stock market situation and the like, which are required to be replaced by the latest information with the lapse of time, are stored in a buffer memory BM included in the output section as  
10 described later. As a result, the information can be directly transferred to the player without accessing the hard disk memory HDD on each occasion. Also, the music program, if large in sales amount, may be stored in the buffer memory BM. In this case, the top ten items in  
15 sales volume of each music category may be displayed as a display menu to facilitate selection by the user.

[0013]

The output section of the terminal device includes an output interface OUTINF connected to the VME  
20 bus, a player controller PCTL, a buffer memory BM, a monitor controller MOCTL, a monitor MONT, etc, as shown in Fig. 4. The output section is connected to the player through a connector for receiving a digital signal as a commodity. The buffer memory BM has a  
25 comparatively large storage capacity of approximately 96 MB, which is equivalent to about ten times as large as the maximum storage capacity 8 MB of the player as described later.



1           The monitor MONT, though not specifically  
limited, has a speaker and a headphone output and is  
used for reproducing a starting part of a given music  
selected from the music program. This function is one  
5 like reading a book while standing in bookstore, and is  
effective to promote the sale of the invisible digital  
signal or prevent an error in selection of the digital  
signal. The output function of the monitor, though not  
specifically limited, is activated during about ten  
10 seconds as a maximum time length only when the touch-key  
or the like is turned on. As a result, the monitor  
output is stopped as soon as the object of the selection  
is achieved, and therefore the wasted time of monitor  
playback is eliminated. The monitor MONT and the  
15 monitor controller MOCTL used in this configuration are  
equivalent to those used in the playback circuit of the  
player described later.

[0014]

As explained above, commodities including  
20 cigarettes and juice sold by the vending machine are  
encased in a package or a container integrally  
therewith. Commercialized information or the like, on  
the other hand, are sold by use of prints with paper or  
a floppy disk or an IC memory as a medium functioning as  
25 a package or a container. A music program is also  
offered for sale in a form integrated with a storage  
medium such as magnetic tape or compact disk. These  
media have no commercial value of their own. Only in

1 combination with an "electronic notebook", a personal  
computer or the like terminal device, information is  
retrievable and processed as a commodity. Also, the  
value of a music program as a commodity is exhibited  
5 only in combination with a cassette tape recorder or  
other reproducing device.

In contrast, according to the present  
invention, a digital signal as a commodity is received  
in the form of electrical signal without any  
10 intermediary of a storage medium functioning as the  
container mentioned above. For the purpose of receiving  
of the digital signal in the form of electrical signal,  
a memory circuit RAM is mounted on the player as  
described later. A digital signal introduced to this  
15 memory circuit RAM can be reproduced through a playback  
circuit of the player as a unit. Specifically, the  
received commodity directly exhibits the value thereof  
as a commodity. These two features make the present  
invention conspicuously different from the conventional  
20 commodity transactions. Further, according to a system  
in which the player is connected to the terminal device  
and in which a digital signal is transmitted and  
received as a commodity as described above, only the  
required information can be specified and sold when  
25 required.

[0015]

In Fig. 4, POW designates a power supply,  
which, though not specifically limited, supplies

1 power from the terminal device to the player for the  
purpose of transmitting a high-speed digital signal,  
i.e., writing operation. Also, in the case where a  
rechargeable secondary battery is used as a power supply  
5 of the player in place of the primary battery, as  
described later, or in the case where primary and  
secondary batteries are built in, a digital signal is  
transferred when the player is connected to a server.  
At the same time, the secondary battery is charged  
10 rapidly by the power supply POW. Signals transferred  
between the output section and the player are an  
operating voltage V, a digital signal D, an address  
signal A, a control signal C or a status signal S, etc.

[0016]

15 A block diagram of an embodiment of the player  
is shown in Fig. 5.

The player is roughly comprised of a large-  
scale integrated circuit LSI constituted by a gate  
array, a memory circuit RAM for storing a digital  
20 signal, and a playback circuit. The memory circuit RAM,  
though not specifically limited, includes a pseudo-  
static RAM (PSRAM) having a storage capacity of about 8  
MB. As described later, for example, sixteen pseudo-  
static RAMs of about 4 megabits are mounted to realize  
25 the storage capacity of about 8 MB described above. The  
large-scale integrated circuit LSI has mounted thereon a  
controller CTL, an address counter AC, a multiplexer MPX  
and a parallel-to-serial converter P/S. The controller

1 CTL forms various control signals for read-and-playback  
operations of the digital signal stored in the memory  
circuit RAM and a control signal used for data input to  
the memory circuit RAM.

5 The address counter AC generates an address  
signal for reading the digital signal stored in the  
memory circuit RAM. The multiplexer MPX switches  
between the address in accessing the memory circuit RAM  
from the server (terminal device) and the address in  
10 accessing the memory circuit RAM inside thereof. More  
specifically, a digital signal is written into the  
memory circuit RAM in accordance with the address from  
the server side, while information is read for playback  
operation of the particular digital signal in accordance  
15 with the address generated from the address counter AC.

[0017]

LPF designates a low-pass filter including a  
digital filter circuit for inputting only the band  
component required for playback to the digital-to-analog  
20 converter. According to this embodiment, as described  
later, a digital signal of a plurality of sampling rates  
is handled in accordance with the information or program  
involved. The pass band of the digital filter is  
switched in accordance with these sampling rates. The  
25 digital-to-analog converter has the function of  
outputting analog signals for the right and left  
channels so separated in accordance with the stereo  
signals inputted in time division. In the case where

1 the digital signal is monaural, the same analog signal  
is outputted from the two channels. The player is  
adapted to generate an audio output from the headphone  
in order to reduce the size and weight thereof. Outputs  
5 R and L designate a headphone terminal.

[0018]

A plan view of an embodiment of the packaging  
board configuring the player is shown in Fig. 6. The  
player includes a control board and a memory board. The  
10 control board has mounted along the longitudinal ends  
thereof a power supply section with button cells  
inserted therein and a connector section. The board  
surface between the power supply section and the  
connector section has mounted thereon electronic parts  
15 such as semiconductor integrated circuit devices or the  
like making up the large-scale integrated circuit LSI,  
amplifier devices AMP1, AMP2, a low-pass filter LPF and  
a digital-to-analog converter DAC. The connector is  
conforming to the JEIDA standard (a standard for memory  
20 card and the like). The power supply section includes  
button cell holders and can be packaged with four alkali  
button cells (LR44), for instance. The size of this  
control board, though not specifically limited, is set  
to 52 mm by 82 mm so as to be accommodatable in the  
25 existing IC card case.

The memory board covers the area other than  
the comparatively thick parts of the connector section  
and the power supply section of the control board, and

1 has mounted eight PSRAMs on each side thereof. The  
memory board and the control board are connected with  
each other by a flexible wiring board. In other words,  
the two boards are openable in two directions, right and  
5 left, to facilitate inspection and repair.

[0019]

Fig. 7 shows a side view of the package board  
as housed in a case. The memory board is folded over  
through the flexible wiring board on the surface area of  
10 the control board other than the power supply section  
and the connector section. As a result, the accommoda-  
tion in a case equivalent to the existing IC card (RAM  
card) is made possible, while at the same time realizing  
a small, thin player. Also, since the memory board and  
15 the control board can be opened at the time of repair as  
described above, the electronic parts such as IC and LSI  
can be easily replaced.

[0020]

Fig. 8 is a plan view showing another embodi-  
20 ment of the player 101.

In this embodiment, the body of the player and  
the memory section are detachable. Specifically, the  
body of the player includes, as in the case mentioned  
above, a control board having thereon such ICs as a  
25 large-scale integrated circuit for control operation, a  
digital-to-analog converter DAC and an amplifier, a  
battery case and a memory card connector based on the  
JEIDA standard. As shown by dotted line in the drawing,

1 there is provided an internal space for insertion of the  
memory section (memory card) in the form of thin card  
and a memory section connector shown in Fig. 8. The  
memory section has a pseudo-static RAM and a backup  
5 battery housed in a card-like thin plastic case, for  
example, as mentioned above. By making the memory  
section detachable in this way, a plurality of types of  
memory card are made available. A variety of RAMs  
including the static RAM and dynamic RAM or the same  
10 type of RAM having a plurality of different storage  
capacities may be prepared. Also, in addition to these  
RAMs, the ROM card may be used. Not only the mask-type  
ROM but also EEPROM may be used for receiving digital  
signals. In the case where the EEPROM is used, the  
15 receiving of a digital signal, that is to say, the write  
operation thereof takes a little longer time than when  
the RAM is used. Nevertheless, the use of the backup  
battery is eliminated, thereby simplifying the produc-  
tion and handling of the memory card.

20 [0021]

Fig. 9 is a block diagram showing an  
embodiment of the body of the player and the memory  
section.

A memory card connector based on the JEIDA  
25 standard to be connected with the information server as  
described above is arranged on the outside of the body  
of the player. The player has a memory section

1 connector built therein. The card-like memory section  
is detachable through these memory section connectors.

The data inputted from the memory card  
connector corresponding to the information server is  
5 supplied to a data input terminal Di of the memory  
section through the memory card connectors. The address  
inputted from the memory card connector corresponding to  
the informatoin server is supplied to an input A of the  
selector. The other input B of this selector is  
10 supplied with a playback address generated by the memory  
address generator at the inside of the player. The  
address for receiving of a digital signal or the  
playback address is selectively supplied to the address  
terminal A of the memory section through the selector.  
15 The control signal inputted from the memory card  
connector corresponding to the information server is  
supplied to the input A of the selector. The other  
input B of the selector is supplied with a playback  
control signal generated by the controller of the body  
20 of the player. The control signal for receiving of the  
digital signal and the playback control signal is  
selectively supplied to the control terminal C of the  
memory section through the selector.

[0022]

25 In the manner mentioned above, the selectors  
are provided for switching the addresses or the control  
signals so as to selectively perform one of the  
receiving of the digital signal in accessing the memory



1 section from the information server side and the  
playback of the digital signal in accessing through the  
memory address generator or controller 1101 inside of  
the player. In this playback operation, the digital  
5 signal outputted from the output terminal Do upon the  
read operation of the memory section is outputted as an  
audio signal through the memory section connectors and a  
playback circuit including the low-pass filter LPF, the  
digital-to-analog converter DAC and the amplifier inside  
10 of the player.

The controller inside of the player is adapted  
to control the digital-to-analog converter DAC and the  
low-pass filter LPF mentioned above in accordance with  
the ID code or the like of the reproduced digital  
15 signal.

The power supplied from the information  
server, on the other hand, is used also as an operating  
voltage for high-speed writing of the digital signal  
into the memory section connected through the memory  
20 sections, or for rapid battery-charging operation in the  
case where the batteries are mounted inside of the  
player as the secondary batteries.

[0023]

A block diagram of an embodiment of the power  
25 supply system for the player is shown in Fig. 10. The  
player, as described above, is comprised of a memory  
circuit RAM, a controller CTL made up of a digital  
circuit, a digital filter LPF, a digital-to-analog

1 converter DAC and an amplifier AMP for outputting an  
analog signal. Each of these circuit blocks has a  
different operating voltage. The memory circuit RAM,  
for instance, requires a comparatively high operating  
5 voltage of about 4 V when a pseudo-static RAM is used as  
mentioned above. In contrast, the use of a CMOS circuit  
gate array or the like in a digital circuit makes  
possible an operation at a comparatively low voltage of  
about 3 V. The amplifier circuit AMP for driving the  
10 headphone is operable even at a lower operating voltage  
of about 1.5 V. As a result, except for the memory  
circuit RAM, which is supplied steadily with a voltage  
from the battery E1, for holding information, the  
voltages of the batteries E2 and E3 are supplied to each  
15 corresponding circuit through the power switches S2 and  
S3 by use of the batteries E1, E2 and E3 adapted for the  
operating voltages of the respective circuits.

[0024]

In this way, the battery life is lengthened by  
20 supplying power to the directly associated circuits by  
use of a plurality of types of batteries having  
different voltage values. If the internal power supply  
is set to the highest voltage of 4 V, for instance, a  
wasteful current flows in the digital or analog circuit  
25 AMP, thereby to increase the current consumption. If  
the voltage of 4 V is supplied through an internal  
voltage drop circuit, the current consumption in the  
voltage drop circuit would shorten the battery life.

1 According to the present embodiment, in contrast, power  
is supplied through a selected battery having the  
required minimum capacity for each circuit, and  
therefore the wasteful current consumption is decreased,  
5 thereby substantially lengthening the battery life.

[0025]

If the writing of a digital signal into the  
memory circuit RAM or the reading of a digital signal  
therefrom is to be speeded up, the operating current of  
10 the memory circuit must be increased. For this purpose,  
the information server is provided with power supplying  
connectors for supplying an operating voltage of about 5  
V higher than the internal voltage. In this case, in  
order to automatically switch the power between the  
15 battery and the server sides, the connector and the  
battery E1 are used to supply a voltage to the power  
terminal of the memory circuit RAM through diodes D1 and  
D2, respectively. In this configuration, once the  
player is connected to the server, the diode D1 is  
20 turned on since the operating voltage of the server is  
about 5 V and higher than the voltage of about 4 V  
across the battery E1, and the memory circuit RAM is  
operated by the operating voltage from the server side.  
At the same time, the diode D2 on the battery E1 side is  
25 reversely biased into an off state with the result that  
no reverse current flows from the connector of the  
server to the battery E1. When the player is pulled off  
from the server, the connector is opened and therefore

1 the diode D2 is turned on, thereby supplying the voltage  
across the battery D1 to the memory circuit RAM. By  
employing a power supply system of this type, the data  
transfer from the information server to the memory  
5 circuit RAM can be effected at a high speed, while  
lengthening the battery life of the player at the same  
time.

[0026]

Fig. 11 shows a format of a digital signal  
10 transferred from the terminal device to the player  
according to an embodiment.

Among some sources of digital signals, a music  
program requires a broad frequency band while news does  
not require such a broad frequency band. In other view  
15 points, stereo signal reproduction is required or  
monaural signal reproduction is sufficient. In this  
way, the limited storage capacity of the memory circuit  
built in the player needs to be utilized effectively in  
accordance with the source, so that a sampling rate, bit  
20 length and stereo/monaural mode of a digital signal can  
be selected depending on the source. This requires the  
setting of the playback conditions corresponding to each  
source. In this case, if manual selection is attempted,  
display means used for designating the selection would  
25 be added, with the result that the operation by an  
unaccustomed user would extremely deteriorate the sound  
quality or make playback impossible because of mismatch  
of the playback conditions against the source.

1

[0027]

In order to solve this problem, an ID code for designating the playback conditions is inserted in the head of a digital signal as shown in Fig. 11. This ID code is followed by a data including a digital signal to be reproduced. In this way, a digital signal and the ID code for designating the playback conditions are delivered to the player as an integral signal. As a result, the ID code and the digital signal are integrally stored in the memory circuit RAM of the player. In the case of employing a system for transferring the ID code separately from the digital signal to the player, some idea would be needed to prevent disappearance of the ID code when the power for the player is interrupted. This problem, however, is not posed when the digital signal is stored integrally in the memory circuit as described according to the present embodiment.

20

[0028]

A block diagram of an embodiment of the player corresponding to a digital signal into which the ID code is inserted is shown in Fig. 12.

The digital signal first read from the memory circuit RAM is taken into a register REG by being regarded as the ID code. Of all the ID codes taken into the register REG, the bits D0 and D1 are inputted to the selector SEL, so that a clock pulse corresponding to the sampling rate among four clock pulses formed by the

1 clock generator CPG is selected and transmitted to the  
controller CTL. The clock generator CPG forms four  
clock pulses corresponding to the sampling rates in  
response to a reference frequency signal formed by the  
5 oscillator OSC.

Also, the bit D2 is inputted to a bit length  
converter. The bit length converter has the function of  
parallel-to-serial conversion and inputs to a low-pass  
filter LPF a digital signal outputted from the memory  
10 circuit RAM in maximum units of two bytes in accordance  
with the bit length designated by bit D2. The low-pass  
filter LPF, including a digital filter, receives a clock  
pulse corresponding to the sampling rate from the  
controller CTL and cuts an extraneous frequency band of  
15 the input digital signal. Also, the digital-to-analog  
converter DAC converts an input digital signal into an  
analog signal in response to a clock pulse corresponding  
to the sampling rate from the controller CTL. The  
analog amplifier AMP is for amplifying the analog signal  
20 thus converted thereby to form a drive signal such as  
for headphone. Although not shown in the drawing, the  
output section of the digital-to-analog converter DAC  
has a low-pass filter including a resistor and a  
capacitor.

25 [0029]

The ID code, though not specifically limited,  
includes eight bits of D0 to D7, of which D0, D1, for  
instance are used to designate four sampling

1 frequencies. The frequency 5.5125 kHz is designated  
when D0 and D1 are 00, 11.025 kHz when D0 and D1 are 01,  
22.05 kHz when D0 and D1 are 10, and 44.1 kHz when D0  
and D1 are 11. Bit D2 is used for designating the  
5 resolution. Eight bits are designated when it is 0, and  
16 bits when it is 1. On the other hand, bit D3 is used  
for mode designation, setting "monaural" when it is 0  
and "stereo" when it is 1. The remaining four bits D4  
to D7 are reserved for extension.

10               The relationship between the memory capacity  
(total number M of bits) of the memory circuit RAM, the  
bit length N as a resolution, the sampling rate  $f_s$ , the  
mode S (assuming that stereo  $S = 2$  for stereo mode, and  
 $S = 1$  for monaural mode) and the recording/playback time  
15 t is expressed by equation (1) below.

$$t = M / (N \times f_s \times S) \quad \text{.....} \quad (1)$$

[0030]

As the sampling rate mentioned above, though  
not specifically limited, 44.1 kHz is used for playback  
of an ultra HiFi music program equivalent to the compact  
20 disk player, 22.05 kHz for playback of a HiFi music  
program, 11.024 kHz for playback of an information  
program such as news, and 5.5125 kHz for playback of an  
automatic answering telephone set, or the like. As  
described above, if the sampling frequency is set in  
25 units of double, the player may form one reference

1 frequency corresponding to say, 44.1 kHz, and by divid-  
ing it in units of  $1/2$ , can easily form the sampling  
frequency. As a consequence, the recording/playback  
time is lengthened in reverse proportion to the four  
5 sampling frequencies  $f_s$  described above. In other  
words, if a predetermined recording/playback time is to  
be obtained, the storage capacity is increased in  
proportion to the sampling rate  $f_s$ .

[0031]

10 In the case where the bit length is increased  
from 8 to 16 bits, the recording/playback time is  
doubled as will be seen from equation (1) above. With  
the increase in bit length, a double storage capacity is  
required of the memory circuit RAM to meet the increase.  
15 If the bit length is reduced to 8 bits, by contrast, the  
recording/playback time is increased to double for the  
same storage capacity. In stereo mode, specifically, a  
double data is required as compared with when the system  
is in monaural mode. More specifically, in stereo mode  
20 when right and left signals are outputted alternately  
from the memory circuit RAM, the required storage  
capacity doubles from that required in monaural mode.

According to this embodiment, the three  
playback conditions including sampling rate, bit length  
25 and mode are set for a digital signal source as  
described above, and are combined as desired to permit  
playback, whereby the limited storage capacity of the  
memory can be utilized to the maximum efficiency. The



1 playback conditions which can be combined in a great  
variety can be automatically set in the player by the  
use of the ID code, and therefore any user can easily  
reproduce the information received without any operating  
5 inconvenience.

[0032]

The type or frequency of the sampling rate can  
be set as desired. In such a case, an arrangement  
should be made to generate a clock pulse in accordance  
10 with each sampling rate. Also, the ID code may have  
added thereto a bit that can be designated by the  
operation of a terminal device. The slow or fast  
playback mode may be automatically set by means of the  
remaining bits as explained later, for example, or a  
15 playback mode such as reproduction by program or  
continuous reproduction for the whole program may be  
designated automatically.

[0033]

Fig. 13 is a circuit diagram showing an  
20 embodiment of a quantizing noise remover.

When an analog signal is quantized, a quantiz-  
ing noise (error component) is always generated. This  
quantizing noise is offensive to the ear especially  
during a voice interval. According to the present  
25 embodiment, a quantizing noise remover as described  
below is inserted in the input of the digital-to-analog  
converter DAC.

1

[0034]

The digital signal read out of the memory circuit RAM is inputted to the digital-to-analog converter DAC and is converted into an analog signal Vout.

5 The quantizing noise remover according to the present embodiment, though not specifically limited, is intended for a case in which a digital signal is comprised of a 2' complement binary code. The digital signal including D0 to Dn read out of the memory circuit RAM is inputted  
10 to the corresponding input terminals D0 to Dn of the digital-to-analog converter DAC through the AND gates respectively. The digital signal read out of the memory circuit RAM is inputted to a level checker shown by dashed line for checking a level where the signal is  
15 considered to represent a voice interval. The output signal which has been considered to represent a voice interval by this level checker is inputted to a timer shown by dashed line in the same drawing for time judgment. If the level considered to represent a voice  
20 interval by the level checker and the timer continues for a predetermined time length, the particular period is decided to be a voice interval, so that the output from an inverter becomes a logic zero, thereby controlling the system to close the AND gates. Specifically,  
25 the AND gates forcibly set the signals D0 to Dn inputted to the digital-to-analog converter DAC to logic 0 by the logic 0 of the output signal of the inverter without

1 regard to the digital signal read out of the memory  
circuit RAM.

[0035]

The digital signals D0 to Dn are comprised of  
5 2' complement binary codes as explained above. More  
specifically, when D0 to Dn are eight bits, the positive  
maximum value takes 01111111 and the negative maximum  
value 10000000, with the "0" level as 00000000. +1 in  
decimal notation is equivalent to 00000001 in binary  
10 notation. Once a time period is considered to be a  
voice interval as described above, therefore, the output  
of the AND gates is fixed to zero, thereby making it  
possible to remove the quantizing noise completely  
during a voice interval.

15 [0036]

The level checker in Fig. 13 is adapted to set  
a positive maximum value  $+\Delta L$  and a negative maximum  
value  $-\Delta L$  considered to represent a voice interval.  
When +1 is assumed to be a positive maximum value  $+\Delta L$ ,  
20 for example, the input B of the comparator CP1 takes the  
form of 00000001, while when -1 is assumed to be a  
negative maximum value  $-\Delta L$ , the input B of the  
comparator CP2 is given as 11111111. The input A of the  
comparators CP1, CP2 is supplied with a digital signal  
25 from the memory circuit RAM. A "1" output signal is  
formed by the comparator CP1 when  $A \leq B$ , and by the  
comparator CP2 when  $A \geq B$ . The output signals of these  
comparators CP1 and CP2 are outputted through the AND

1 gate. As a result, the output of the AND gate is "1"  
detecting a voice interval when the digital signal is  
00000001, 00000000 or 11111111.

When the digital signal is 00000010 or  
5 otherwise larger than  $+\Delta L$ , the output of the comparator  
CP1 is "0", while when the digital signal is 11111110 or  
otherwise smaller than  $-\Delta L$ , the output of the comparator  
CP2 is "0". As a consequence, the AND gate forms a "1"  
output signal only when the digital signal is included  
10 within a range considered to represent a voice interval.

[0037]

The timer includes a counter CNT and a  
comparator CP3. The reset input R of the counter CNT is  
supplied with a detection output of the level checker.  
15 When a voice interval is judged to be involved, the  
reset state of the counter CNT is cancelled, and  
therefore the counting operation of the clock pulses CK  
is started by the counter CNT. The count output of the  
counter CNT is supplied to the input A of the comparator  
20 CP3. The input B of the comparator CP3 is supplied with  
a set time  $t$  for regarding a given period as a voice  
interval. As a result, the comparator CP3 outputs a "1"  
signal ( $A \geq B$ ) when the voice interval level continues  
to exceed the set time  $t$ . This output signal is  
25 inverted at the inverter and is inputted to the AND  
gates, and therefore regardless of the digital signal  
read out of the memory circuit RAM, the digital signal

1 supplied to the input of the digital-to-analog converter  
DAC assumes a "0" level of 00000000.

When the level checker is supplied with a  
level of a digital signal exceeding  $+\Delta L$ , the comparator  
5 CP1 or CP2 detects the fact, and reduces the output to  
"0", thereby resetting the counter CNT of the timer. As  
a result, the output signal of the comparator CP3 of the  
timer becomes "0", so that the control input of the AND  
gates is set to "1" through the inverter. The input of  
10 the digital-to-analog converter DAC is thus supplied  
with a digital signal read out of the memory circuit  
RAM. In this manner, immediately after the end of a  
voice interval, the digital signal read out of the  
memory circuit RAM is converted into an analog signal.

15 [0038]

The result of an experiment conducted by the  
inventor shows that the set time  $t$  of the timer is  
generally desirably in the range from 0.5 ms to 20 ms  
depending on the contents of the music or news program  
20 involved. This range may of course be exceeded to some  
degree in setting a time without any problem. Also, the  
level considered to be a voice interval may be switch-  
able in accordance with the input source or the related  
resolution. In the case of a 16-bit digital signal, for  
25 example, it is generally desirable to set a wider range  
than in the case of a 8-bit digital signal. Also, the  
digital signal of 2' complement binary code need not be  
used, so that in the case of 8-bit digital signal,

1 01111111 or 10000000 may be set at an AC-like neutral  
level. In the case of such a digital signal, the  
digital signal from the memory circuit RAM may be  
replaced by a selection of 01111111 or 10000000 if a  
5 voice interval is detected by a combination of a  
multiplexer and a gate circuit.

[0039]

Waveforms for explaining the operation  
mentioned above are shown in Fig. 14. The waveform A in  
10 the drawing represents a case in which the digital  
signal from the memory circuit RAM is directly inputted  
to the digital-to-analog converter to form an analog  
signal. As shown in Fig. 14, the signal undergoes a  
change in accordance with the quantizing error during a  
15 voice interval, thus generating a noise cacophonous to  
the ear. In the quantizing noise remover according to  
the present embodiment, in contrast, as shown by B in  
Fig. 14, upon the lapse of a predetermined time  $t$   
considered to be a voice interval, a digital signal  
20 corresponding to "0" level is forcibly subjected to  
digital-to-analog conversion by the AND gates, and  
therefore the above-mentioned noise continues to be  
outputted until the arrival of the next "0"-level audio  
signal free of the noise. The predetermined time length  
25  $t$  is very short and ranges from about 0.5 ms to 20 ms,  
and therefore the quantizing noise generated during this  
period is not offensive to the ear.

1           The quantizing noise remover according to the  
present embodiment is not only used with the player as  
described above but also finds wide applications as  
various digital audio processors such as a digital audio  
5 tape recorder for processing a digital audio signal.

[0040]

Fig. 15 is a circuit diagram showing an  
embodiment of a security circuit used with a digital  
signal selling system according to the present  
10 invention.

In selling a digitized audio information, etc.  
as a commodity, it is important to prevent it from being  
easily duplicated in order to improve the commercial  
value thereof. For this purpose, a first method is to  
15 add the function of permitting only a specified person  
to perform the substantial playback operation of the  
digital signal. In a second method, upon transfer to  
the player of a digital signal sold in the digital  
signal selling system according to the above-mentioned  
20 embodiment, the signal conversion described below is  
effected within the player 101 as a function to prevent  
ready duplication.

[0041]

In order to permit only a specified person to  
25 perform the playback operation or to duplicate, the read  
output section of the memory circuit RAM is provided  
with EOR gates controlled by a password check signal.  
These EOR gates may be either provided as parts

1 corresponding to all bits of the read signals D0 to Dn  
or only for one or a plurality of bits including at  
least the most significant bit with equal effect.

The input data terminal of the memory circuit  
5 RAM is supplied directly with a digital signal trans-  
ferred from the terminal device server. In the case of  
using a semiconductor memory with the input and output  
of the memory circuit RAM shared with each other, the  
EOR gates are inserted in the read signal route of the  
10 signal bus connecting the data terminal of the memory.  
The digital signal is read out of the memory circuit RAM  
by an address signal generated by the address counter AC  
receiving an address update pulse.

[0042]

15 The password described above is set in advance  
in the player by a switch, ROM, etc. This password is  
notified to the purchaser at the time of purchase of the  
player by him. As a result, the password is set at the  
time of reproducing the digital signal by the player.

20 When the password registered by a comparator or the like  
not shown coincides with the password inputted, a  
password judging signal is reduced to "0". The EOR  
gates thus output a "0" coincidence signal when "0"  
coinciding with "0" is inputted thereto. When "1"  
25 signal not coincidental with "0" is inputted, on the  
other hand, a "1" noncoincidence signal is outputted.  
In this way, when the password judging signal is "0",



1 the EOR gates output an input digital signal in its direct form.

[0043]

When it is judged by a comparator, etc. not  
5 shown that a registered password fails to coincide with the input password, by contrast, the password judging signal of "1" is outputted. As a result, the EOR gates output a "0" coincidence signal when a "1" signal coinciding with "1" is inputted thereto, and a "1" noncoincidence signal when "0" not coinciding with "1" is inputted thereto. In this fashion, when the password judging signal is "1", the EOR gates output an input digital signal in an inverted form. When the EOR gates are inserted for the digital signals of all the bits as  
15 explained above, all the bits are inverted when the passwords fail to coincide with each other, so that the resulting audio signal with inverted bits, which is meaningless if converted into an analog signal, assures the confidentiality of information. Also, a password is  
20 required even when taking a copy, or, in other words, even when the data is outputted outside from the memory circuit RAM, thus preventing an easy duplication.

[0044]

Some information such as news or traffic data  
25 are too small in importance to protect. In such a case, the password may be made null and void by use of the ID code mentioned above. In other words, the system may be arranged to perform the above-mentioned security

1 operation on condition of coincidence of the password,  
only when information protection is required by the ID  
code. By doing so, the seller may designate an item  
requiring security. Also, a call received by the  
5 automatic answering telephone set may be of such a  
nature that one wants to keep it private. In such a  
case, an arrangement may be made to designate security  
mode by the ID code to assure protection by the terminal  
device. In any way, the operating trouble is minimized  
10 by making such an arrangement as to require a password  
input only when true information protection is assured  
by the ID code 1308.

[0045]

Fig. 16 is a circuit diagram showing another  
15 embodiment of the security circuit used with the digital  
signal selling system according to this embodiment.  
According to this embodiment, a security circuit using a  
password coincidence signal and EOR gates is inserted in  
the data input terminal side of the memory circuit RAM.  
20 Also in this case, when the passwords are not  
coincident, each bit or one or a given number of bits of  
the digital signal written in the memory circuit RAM are  
inverted and converted into a meaningless audio signal,  
thus assuring the confidentiality as in the afore-  
25 mentioned case. In this case, at the time of transfer  
of the digital signal requiring security from the  
terminal device, a data is transferred substantially  
effectively only when a password is inputted and is

1 coincidental by the operation of touch keys of the  
terminal device, while if the password is incoincident,  
the bits are inverted as mentioned above, thereby  
transferring a substantially meaningless digital signal.  
5 As an alternative, the transfer operation itself may be  
suspended.

[0046]

Fig. 17 is a circuit diagram showing still  
another embodiment of the security circuit used with a  
10 digital signal selling system according to the present  
invention. According to this embodiment, a security  
circuit using a password coincidence decision signal and  
an exclusive OR circuit EOR is disposed on the address  
input terminal side of a memory RAM. In this case, when  
15 the password fails to coincide, unlike when the address  
selection of the memory RAM is an input, one or a  
plurality of bits are reversed, so that successive  
addresses of the input are changed to discrete output  
addresses. As a result, a digital signal read against  
20 this discrete address is meaningless any longer as audio  
information, thus assuring security as in the  
aforementioned case.

The embodiment of Fig. 15 or Fig. 16 may be  
combined with that of Fig. 17 to configure a security  
25 circuit including one or a plurality of EOR gates for  
data and address respectively. In this way, the  
combination of data and the related address makes  
tighter information protection possible.

1

[0047]

Fig. 18 is a circuit diagram showing a further embodiment of the security circuit used with a digital signal selling system according to the present invention. This embodiment is mainly aimed at preventing duplication of a digital signal. The player has passwords registered therein by EPROM or the like. These passwords are codes not notified even to the purchaser of the player.

10

Each bit of these codes is supplied to one of the inputs of the EOR gates inserted in the input and output of the memory circuit RAM. In Fig. 18, an EOR gate is provided for all the bits of the data input and output of the memory circuit RAM. Instead, the EOR gates may be inserted for only a given one or a plurality of bits. Each corresponding input and output, however, are provided as a pair with EOR gates respectively.

15

[0048]

20

The data input bit for which the input of the EOR gates have been reduced to "0" by the above-mentioned password is written directly, while the data input bit for which the input of the EOR gates has been made "1" by the above-mentioned password is written in inverted form.

25

The digital signal read out of the memory circuit RAM is applied through the EOR gates controlled by the above-mentioned same password, whereby the

1 through bits remain through, while inverted bits are  
inverted again into the original form. As a result, the  
same digital signal as an input digital signal is  
transmitted to the digital-to-analog converter DAC,  
5 thereby posing no problem in audio playback.

[0049]

In contrast, the reading itself of the memory  
circuit RAM is outputted to the connector side of the  
player. In other words, a digital signal bit-converted  
10 by the password is outputted on the write circuit side.  
As a result, a copied digital signal, unlike the  
original digital signal, becomes a meaningless one, and  
therefore the duplication is substantially prevented.  
By the way, the password may be comparatively easily  
15 decoded by any person having the knowledge of digital  
circuits. In view of the selling price of the news,  
stock market news or the music program mentioned above,  
however, the labor required for destroying the security  
would be higher and more meaningless. Specifically, the  
20 security in the digital signal selling system according  
to this invention is sufficient if an easy duplication  
or eavesdropping can be prevented.

[0050]

Fig. 19 is a circuit diagram showing still  
25 another embodiment of the security circuit used with the  
digital signal selling system according to the present  
invention. In this embodiment, instead of the EOR gates  
for passing a signal in direct or inverted form, a bit-

1 rearranging circuit is used. The bit-rearranging  
circuit has two signal routes, one for outputting an  
input signal in its direct form, and the other for  
spatially exchanging the output-side bits D0 to Dn for  
5 the input-side bits D0 to Dn. Specifically, the least  
significant bit D0 is outputted as the most significant  
bit Dn, or D1 is outputted as D2. If the password  
judging signal is incoincident, this bit-rearranging  
circuit enables a digital signal to be outputted with  
10 meaningless ones destroyed. This bit-rearranging  
circuit may be inserted on the input-side data in place  
of the EOR gates shown in Fig. 16, or on the address  
input side in place of the EOR gates shown in Fig. 17.

[0051]

15 Fig. 20 is a specific circuit diagram showing  
an embodiment of the bit-rearranging circuit used with  
the above-mentioned security circuit.

In Fig. 20, a bit-rearranging circuit for one  
bit is illustratively shown for a digital signal  
20 including a plurality of bits.

One of input digital signals of a plurality of  
bits including D0 to Dn is selected by a selector and  
outputted as the least significant bit D0 from the  
output terminal. The selector selects and outputs one  
25 of the signals D0 to Dn by a selection signal formed by  
a decoder.

[0052]

In the case where the digital signals D0 to Dn

1 are eight bits, a random number generator generates a 3-bit random number (0 to 7 in decimal notation), which is supplied to the input terminal A of the selector SEL. The other input terminal B of the selector SEL is  
5 supplied with a 3-bit binary signal (000) designating the decimal zero corresponding to the output bit D0. The selection terminal S of the selector SEL is supplied with a password judging signal. The password judging signal becomes a logic "1" when the password is  
10 coincidental, so that the signal of the input B of the selector SEL is sent from the output Y.

[0053]

As described above, when the password is coincidental, the decimal zero corresponding to the  
15 output bit D0 is inputted to the decoder through the selector SEL, and therefore a selection signal of the input bit D0 is formed and supplied to the selector by the decoder. When the password is incoincident, on the other hand, the 3-bit signal generated by the random  
20 number generator is selected and inputted to the decoder. As a result, the decoder decodes a 3-bit signal and forms one selection signal from the 8-bit input signals D0 to Dn. The probability of the input signal D0 being selected is  $1/8$ . Since a similar  
25 circuit is provided also for the remaining 7-bit output signals, the probability of the input signals D0 to Dn being outputted in their direct form even when the password is incoincident is as small as  $1/(8 \times 8 \times 8 \times$

1 8 x 8 x 8 x 8 x 8) = 1/16777216, thus making information  
protection possible. The feature of this circuit lies  
in that since the random number generator makes the  
combination of bit exchange different in each case, it  
5 is substantially impossible to decode true data from the  
bit train outputted.

[0054]

Fig. 21 is a block diagram showing an embodi-  
ment of a digital audio signal processor for realizing  
10 fast and slow playback with high sound quality.

According to the digital signal selling system  
mentioned above, fast playback is considered effective  
for listening to such information as news and various  
market situations in short time. In the case where the  
15 player user is an aged person or the like, on the other  
hand, it is considered effective to add the slow play-  
back function in view of the fact that the hearing  
ability is deteriorated and it takes some time before  
the language is understood.

20 In an analog-type recording system such as the  
conventional cassette tape recorder, the tape speed may  
be changed to assure slow or fast playback by changing  
the playback time as compared with the recording time.  
When the tape speed is changed this way, however, the  
25 pitch (frequency) is also undesirably changed, resulting  
in the loss of fidelity to the original sound, thereby  
making it very hard to listen to.



1           On the other hand, the playback speed may be  
changed without changing the pitch by the use of the  
signal processing technique using a digital signal  
processor or the like. In such a system, however, the  
5 configuration is complicated with an increased power  
consumption, with the result that it cannot be mounted  
on the portable player and at the same time the cost is  
very high. Further, such a system is effective only for  
voice and the reproduction of a music program is  
10 difficult.

[0055]

          According to the present embodiment, the voice  
interval contained in the audio information is utilized  
in such a manner that the voice interval is shortened or  
15 substantially deleted for fast playback and enlarged or  
extended for slow playback. By employing this system, a  
high sound quality is maintained since the pitch of the  
original sound remains unchanged in both fast and slow  
playbacks. In addition, this configuration, as des-  
20 cribed later, is realizable with a comparatively simple  
combination of logic circuits without using any expen-  
sive, complicated devices like the digital signal  
processor, thus making possible a system low in price  
and small in size.

25           [0056]

          The embodiment of Fig. 21 concerns a case in  
which the system is mounted on the player of the digital  
signal selling system.

1           The digital audio signal read from the memory  
circuit RAM is inputted to a digital-to-analog converter  
DAC on the one hand and to a voice interval detector on  
the other hand. The voice interval detector may be made  
5 up of a circuit similar to the one used in the  
quantizing noise remover in the embodiment of Fig. 13.  
In the case where the quantizing noise remover is also  
incorporated, the voice interval detector may be shared  
therewith in operation. The output signal of the voice  
10 interval detector is inputted to a fast/slow playback  
circuit. The fast or slow playback is designated for  
the fast/slow playback circuit under the control signals  
of modes 1 and 2. This fast/slow playback circuit  
controls the operation of the address counter AC for  
15 forming a read address signal of the memory circuit RAM  
in response to a mode signal. When the fast playback is  
designated by mode 1, for example, the clock frequency  
is increased beyond normal level to increase the speed  
of reading the memory circuit RAM during a voice  
20 interval which may be detected, thus substantially  
shortening the voice interval to achieve fast playback.

[0057]

Assume that the slow playback is designated by  
mode 2. When a voice interval is detected, the clock  
25 frequency is decreased below normal level or suspended  
for a predetermined length of time thereby to enlarge or  
extend the read time for the memory circuit RAM during  
the voice interval, thus achieving the slow playback.

1 The output signal of the address counter AC is inputted  
to the memory circuit RAM through the selector. When a  
digital signal is written into the memory circuit RAM,  
the selector causes an external address signal to be  
5 inputted to the memory circuit RAM, while when a digital  
signal stored in the memory circuit is read, i.e., at  
the time of playback of the digital signal, the address  
signal generated by the address counter AC is inputted  
to the memory circuit RAM.

10 [0058]

Fig. 32 is a block diagram showing a specific  
embodiment of the fast playback circuit.

According to this embodiment, the output  
signal of the voice interval detector is supplied  
15 through an inverter N to an AND gate G. This AND gate G  
is for inputting the digital signal from the memory  
circuit RAM to a digital-to-analog converter DAC, and is  
configured the same way as the quantizing noise remover.  
Specifically, this embodiment is intended to achieve the  
20 fast playback while at the same time eliminating the  
quantizing noises during the same interval.

The output signal of the voice interval  
detector is inputted to the control terminal S of the  
selector SEL. The selector SEL is adapted to input two  
25 clock pulses CK1 and CK2 selectively to the address  
counter AC in accordance with the output signal of the  
voice interval detector inputted to the control terminal  
S. The clock pulse CK1, for example, is one

1 corresponding normally to playback, and is adapted to  
have a frequency corresponding to the sampling rate of  
the digital signal. The clock pulse CK2, by contrast,  
is used for fast playback and has a frequency about ten  
5 times higher than the clock pulse CK1.

[0059]

As long as the fast playback is designated,  
upon judgement of a voice interval by the voice interval  
detector, the output signal is raised to high level  
10 (logic "1"). In response to this, the output signal of  
the inverter N is reduced to low level (logic "0"), and  
the AND gate G is closed. In the case of a digital  
signal of 2' complement binary code as mentioned above,  
therefore, the digital signal inputted to the digital-  
15 to-analog converter DAC during a voice interval is  
forcibly made to correspond to the "0" level. Also,  
with the rise of the output signal of the voice interval  
detector to high level, the selector SEL inputs the  
clock CK2 instead of the clock CK1 to the address  
20 counter AC. As a result, the address counter AC updates  
the address at the rate ten times higher than in normal  
playback operation. The voice interval is thus  
shortened to about one tenth, thus assuring fast  
playback equivalently.

25 An experiment conducted by the inventor shows  
that the voice interval accounts for a comparatively  
long time or 30% to 50% of every type of conversation or  
lecture as well as the news program in which a text is

1 read. By eliminating this voice interval virtually, the  
playback time can be shortened to about  $2/3$  to  $1/2$ .

[0060]

At the end of a voice interval, the normal  
5 playback is immediately restored, and therefore the  
sound quality remains the same as the original sound,  
thereby making it very easy to listen to. In the case  
where the fast playback is to be stopped in the circuit  
according to the present embodiment, the only thing  
10 required is to input the output signal of the voice  
interval detector to the control terminal S of the  
selector SEL through the AND gate and the like newly  
added. When no fast playback is desired, on the other  
hand, the input to the AND gate is reduced to "0".  
15 Then, the control terminal S of the selector SEL is  
always kept at low level, so that the clock CK1 is  
inputted to the address counter AC even during a voice  
interval and a voice interval level is outputted for a  
time length corresponding to the voice interval. In the  
20 process, the AND gate G functions as a quantizing noise  
remover to prevent a quantizing noise from being  
generated during the particular period.

[0061]

Fig. 23 is a block diagram showing a specific  
25 embodiment of the slow playback circuit.

This embodiment is intended to generate a  
voice interval enlarged in proportion to the true voice  
interval for slow playback. The output signal of the

1 voice interval detector described above is supplied to  
the set input S of a flip-flop FF on the one hand, and  
to one of the inputs of the AND gate G1 on the other  
hand. The other input terminal of the AND gate G1 is  
5 supplied with a clock pulse CK3 for measuring the voice  
interval. The output signal of the AND gate G1 is  
inputted to a voice interval counter. During the period  
when the presence of a voice interval is judged by the  
voice interval detector, the voice interval counter  
10 counts the clock pulses CK3 thereby to conduct a  
counting operation corresponding to the particular voice  
interval. The counter counts the clock pulses CK3  
supplied thereto through the AND gate G2. The voice  
interval counter is for holding information as well as  
15 for measuring the time of the voice interval. The  
counter for counting the same clock pulses CK3 as this  
voice interval information performs the operation of  
reproducing the particular voice interval.  
Specifically, the outputs of the voice interval counter  
20 and the counter are inputted to a comparator CP and the  
resulting coincidence output  $A = B$  is counted by an N  
counter.

[0062]

The N counter is for designating the voice  
25 interval at N times as longer, and though not  
specifically limited, has an N value variable. The N  
counter is of programmable type, and when the count Q  
comes to coincide with N, outputs a coincidence signal Q

1 (= N) and resets the flip-flop FF. This N counter may  
also be realized by using a down counter. Also, an  
arrangement may be made to conduct the down counting  
from the initial value N, and reset the flip-flop FF by  
5 a borrow output when the count reaches zero.

The output signal Q of the flip-flop FF is  
inverted by the inverter N and is used as a control  
signal for the AND gate G having the function of  
neglecting quantizing noises. The output signal Q is  
10 also used for controlling the AND gate G for supplying  
the clock pulse CK3 to the counter and the AND gate G3  
through the inverter N1 at the same time. This AND gate  
G3 functions as a gate for supplying the clock pulse CK1  
selectively to the address counter AC.

15 [0063]

The circuit operation of this embodiment will  
be described. Upon detection of a voice interval at the  
voice interval detector, the AND gate G1 opens to supply  
the clock pulse CK3 to the voice interval counter. As a  
20 result, the voice interval counter counts the clock  
pulses CK3 as long as a voice interval is judged by the  
voice interval detector. When the voice interval  
detector judges that an audio digital signal has been  
inputted, the flip-flop FF is set in synchronism with  
25 the change of the detection signal from high to low  
level, so that the output signal Q becomes high in  
level, and a digital signal associated with the voice  
interval level is supplied to the digital-to-analog

1 converter DAC in place of the digital signal from the  
memory circuit RAM.

In accordance with the change of the output  
signal Q of the flip-flop FF to logic "1", the output  
5 signal of the inverter N1 becomes logic "0", thereby  
closing the AND gate G3. As a consequence, the address  
counter AC is not supplied with any clock pulse CK1, and  
therefore is left to hold the previous address. In  
other words, the reading operation of the memory circuit  
10 RAM is stopped.

[0064]

With the change of the output signal Q of the  
flip-flop FF to logic "1", the AND gate G2 opens, and  
the counter starts to count the clock pulses CK3. When  
15 the count becomes equal to that of the voice interval  
counter, the comparator CP outputs a coincidence signal  
 $A = B$ , thereby energizing the N counter while at the  
same time resetting the counter. When the N counter  
counts the value N as a result of repeating these  
20 processes of operation, the flip-flop FF is reset.  
Specifically, when the voice interval measured by the  
voice interval counter increases N times as large, the  
flip-flop FF is reset. With the resetting of the flip-  
flop FF, the AND gate G3 opens again, and inputs the  
25 clock pulse CK1 to the address counter AC. As a result,  
the reading of the digital signal from the memory  
circuit RAM is substantially restarted. At the same  
time, the AND gate G is opened, and the digital signal



1 thus read is supplied to the digital-to-analog converter  
DAC. Thus the audio signal is outputted again. In this  
configuration, the extension of the voice interval is  
proportional to the voice interval of the original  
5 sound. Therefore, a conversation or lecture is  
accordingly increased in the length of interval and is  
made less offensive to the ear.

[0065]

When a voice interval is counted, the  
10 quantizing noise is outputted as described above. For  
removing this quantizing noise generated during the  
counting of a voice interval, a method is by inverting  
the output signal of the voice interval detector through  
an inverter to control the AND gate G. In such a case,  
15 a three-input AND gate is used as the AND gate G. When  
a voice interval is counted, the quantizing noise is  
eliminated by the output signal of the voice interval  
detector added as above, and by the output signal Q of  
the flip-flop FF while the voice interval is enlarged  
20 subsequently, as described above.

[0066]

Fig. 24 shows waveforms of operation  
associated with the fast playback circuit of Fig. 22.  
The voice intervals Tm1 and Tm2 of the original signal  
25 can be removed substantially by switching the clock  
pulses supplied to the address counter AC during such  
intervals, and therefore the fast playback is made  
possible without changing the pitch (frequency) of the

1 audio signal, i.e., without deteriorating the sound  
quality of the audio signal.

[0067]

Fig. 25 shows waveforms of operation  
5 associated with the slow playback circuit of Fig. 23.  
Since the voice intervals  $T_{m1}$  and  $T_{m2}$  of the original  
signal are enlarged to  $n$  times as large by suspending  
the operation of the address counter AC during the same  
intervals, the slow playback is realized without  
10 changing the pitch (frequency) of the audio signal,  
i.e., without deteriorating the sound quality of the  
audio signal.

[0068]

Fig. 26 is a block diagram showing another  
15 embodiment of the fast playback circuit according to the  
present invention.

In this embodiment, the address-generating  
operation is directly switched by using an adder AC with  
the address counter AC in order to achieve fast  
20 playback. Specifically, the address counter AC includes  
the adder AC and a register REG for receiving a sum  
output  $A+B$  thereof. The output signal  $Q$  of the register  
REG is fed back to the sum input  $A$  on the one hand, and  
is inputted to selector as a read address of the memory  
25 circuit RAM on the other hand.

The other input  $B$  of the adder AU is supplied  
selectively with 1 and a positive integer  $M$  through the  
selector SEL. The control terminal  $S$  of the selector

1 SEL is supplied with an output signal of the voice  
interval detector. The output signal of the voice  
interval detector is supplied also to the AND gate G for  
eliminating the quantizing noise through the inverter N  
5 as in the aforementioned embodiment.

[0069]

When a voice interval is detected by the voice  
interval detector, the selector SEL selects M in place  
of 1, and transmits it to the adder AU. As a result,  
10 before entering a voice interval, the adder AU performs  
the counting operation by adding +1 to the address  
signal formed by the register 3502 and generating the  
next address signal. When a voice interval is entered  
as mentioned above, the selector SEL inputs M to the  
15 adder AU. As a result, the adder AU adds +M to the  
address signal formed by the register REG to generate an  
address signal skipped by M addresses. Thus the  
address-updating operation during a voice interval is  
equivalently increased in speed, thereby substantially  
20 eliminating the voice interval as in the aforementioned  
embodiments.

[0070]

Fig. 27 is a block diagram showing another  
specific embodiment of the slow playback circuit  
25 according to the present invention.

In this embodiment, a clock pulse CK4 is  
prepared for slow playback. Specifically, in contrast  
to the fast playback circuit shown in Fig. 20, a slow

1 clock pulse CK4 is prepared for slow playback, so that  
when a voice interval is started, the selector SEL is  
switched to select the slow playback clock pulse CK4 in  
place of normal clock pulse CK1. When the frequency of  
5 the clock pulse CK4 is reduced to  $1/N$  in comparison with  
that of the clock pulse CK1, the operation of the  
address counter AC is decreased by a factor of  $N$ ,  
thereby enlarging the voice interval equivalently by a  
factor of  $N$ .

10 In this embodiment, which can be configured  
with a circuit similar to Fig. 22, the input B of a  
selector SEL may be selectively supplied with the clock  
pulse CK2 in fast playback mode and the clock pulse CK4  
in slow playback mode respectively through a similar  
15 selector or an appropriate switching circuit. In this  
way, both the fast and slow playback are made possible.

[0071]

Fig. 28 is a block diagram showing another  
specific embodiment of a slow playback circuit according  
20 to the present invention.

In slow playback mode, the user like an aged  
person feels more convenient to hear as described above.  
If a comparatively long voice interval is enlarged or  
extended, however, the sound becomes difficult to hear.  
25 In view of this fact, the embodiment under consideration  
has added thereto the function of imposing a certain  
limitation on the enlargement or extension of a voice  
interval in slow playback mode.

1 [0072]

According to this embodiment, a circuit described below is added as a basis of the slow playback circuit shown in Fig. 23. The output signal Q of the voice interval counter is supplied to and increased N times as large by a multiplier MU. The N-fold multiplier output is supplied to an input A of a selector SEL and an input A of a comparator CP2. The output signal Q of the voice interval counter is supplied to an input A of a comparator CP3. The other inputs of the selector SEL and the two comparators SP2, CP3 are supplied with a maximum extension time K of the voice interval. The value N for increasing the voice interval by N times or the maximum extension time K, though not specifically limited, can be set within a predetermined range by the player user. The maximum extension time K, though not specifically limited, is adjustable within the range from 1 to 5 seconds. The result of a test hearing in slow playback mode by the inventor shows a proper time length of about three seconds.

[0073]

An input A of the comparator CP1 is supplied with the output signal Q of an extension counter, and the other input B thereof with the output signal Y of the selector SEL. The control terminal S of the selector SEL is supplied with the output signal of the comparator CP2. And the output signals of the

1 comparators CP1 and CP3 are supplied through an OR gate  
CP4 to the reset terminal R of the flip-flop FF, the  
reset terminal R of the voice interval counter, and the  
reset terminal R of the extension counter. The flip-  
5 flop FF is set at the trailing edge of the output signal  
of the voice interval detector, i.e., at the finish  
timing of the voice interval of the original signal, as  
in the previous case. The output signal Q of the flip-  
flop FF is used to control the AND gate G through the  
10 inverter N, supplied to the AND gate G2 for controlling  
the counting operation of the extension counter, and  
also supplied to an AND gate G3 for controlling the  
counting operation of the address counter AC through the  
inverter N1.

15 [0074]

Fig. 29 is a schematic diagram for explaining  
an example of operation of the circuit shown in Fig. 28.  
The original data has a maximum extension time  $T_{max}$   
corresponding to K. Assume that the voice interval  $T_d$   
20 of the original data is larger than the maximum  
extension time K. When the output signal Q of the voice  
interval counter supplied to the input A of the  
comparator CP3 increases beyond the maximum extension  
time K supplied to the input B of the comparator CP3,  
25 the comparator output  $A \geq B$  of the comparator CP3  
becomes logic "1". As a result, the flip-flop FF, the  
voice interval counter and the extension counter are  
reset through the OR gate G4, thereby nullifying the

1 slow playback mode equivalently. The state after the  
slow playback operation thus remains the same as that  
before the slow playback operation. In this way, in the  
case where the voice interval of the original signal is  
5 so long as to fail the object of slow playback as  
mentioned above, the operation of extending the voice  
interval is substantially nullified.

[0075]

Fig. 30 is a schematic diagram for explaining  
10 another example of operation of the circuit shown in  
Fig. 28. In Fig. 30, as in the previous case, the  
original data has a maximum extension time  $T_{max}$   
corresponding to  $K$ . In the case where the voice  
interval  $T_d$  of the original data before processing which  
15 is shorter than the maximum extension time  $K$  becomes  
longer than the maximum extension time  $K$  as a result of  
being increased  $N$  times as long, the comparator  $CP2$   
detects the fact that the voice interval  $T_d \times N$   
determined by the multiplier  $MU$  increases beyond the  
20 maximum extension time  $K$  and sets the comparator output  
 $A \geq B$  to logic "1". In response to the logic "1" state  
of the comparator output signal, the selector  $SEL$   
transmits the maximum extension time  $K$  of the input  $B$  in  
place of the multiplier output  $T_d \times N$  of the input  $A$  to  
25 the comparator  $CP1$ . As a result, when the output signal  
 $Q$  of the extension counter exceeds the maximum extension  
time mentioned above, the output  $A \geq B$  of the compa-  
rator  $CP1$  becomes logic "1", so that the flip-flop  $FF$ ,

1 the voice interval counter and the extension counter are  
reset through the OR gate G4. In this way, the  
processed data is used to limit the extension time of a  
given voice interval to less than the maximum extension  
5 time.

[0076]

Fig. 31 is a schematic diagram for explaining  
still another example of operation of the circuit shown  
in Fig. 28. In Fig. 31, as in the previous cases, the  
10 original data has a maximum extension time  $T_{max}$   
corresponding to  $K$ . In the case where the voice  
interval  $T_d$  of the original data before being processed  
is shorter than the maximum extension time  $K$  and the  
time length  $N$  times the voice interval  $T_d$  is still  
15 shorter than the maximum extension time  $K$  in this way,  
the comparator CP2 detects the fact that the voice  
interval  $T_d \times N$  determined by the multiplier MU is  
shorter than the maximum extension time  $K$ , and sets the  
comparator output  $A \geq B$  to logic "0". In response to  
20 this logic "0" of the comparator output, the selector  
SEL transmits the multiplier output  $T_d \times N$  of the input  
 $A$  to the comparator CP1. As a result, when the output  
signal  $Q$  of the extension counter exceeds the enlarged  
voice interval  $T_d \times N$ , the comparator output  $A \geq B$  of  
25 the comparator CP1 becomes logic "1", so that the flip-  
flop FF, the voice interval counter and the extension  
counter are reset by way of the OR gate G4. In this



1 way, the voice interval is enlarged N times as long in  
the processed data.

[0077]

Fig. 32 shows waveforms for explaining another  
5 embodiment of the fast and slow playback operations.

According to the present embodiment, the data  
compression function is included in addition to the fast  
and slow playback. In other words, the voice intervals  
of the original data are replaced by the voice interval  
10 data MK as shown in the processed signal. In Fig. 32,  
the voice interval data MK represents a point of  
insertion thereof, and at the time of actual analog  
conversion, the part where the voice interval data MK is  
inserted is rendered voiceless. By inserting this voice  
15 interval data MK, the voice intervals are replaced by  
information of several bytes, and therefore the voice  
intervals contained in the digital signal before analog  
conversion are substantially removed. As a consequence,  
the memory capacity required for storing digital signals  
20 can be reduced to about 1/2 to 2/3 or by the proportion  
which the voice interval represents of the whole time  
length. In the case where a data is compressed in this  
way, utilization of the voice interval data MK makes  
slow or fast playback possible by enlarging or  
25 compressing the same signal selectively. This data  
compression may basically use a fast playback controller  
as described above. Although the fast playback  
controller outputs a "0" level signal in order to remove

1 the quantizing noise during a voice interval, the voice  
interval data MK may alternatively be inserted with  
equal effect.

[0078]

5 Fig. 33 is a pattern diagram showing an  
embodiment of the voice interval data MK.

The voice interval data MK includes a voice  
interval mark and a voice interval time data. A  
combination of bit patterns unavailable for a normal  
10 audio digital signal is selected as the voice interval  
mark. According to this embodiment, when the digital  
signal is a 2' complement binary code, a combination of  
a positive maximum value 01111111 and a negative maximum  
value 10000000 is used. A normal audio signal does not  
15 change from a positive to a negative maximum value, and  
therefore this combination is used as a voice interval  
mark. The voice interval mark may alternatively be a  
combination of two, three or four bytes, unlike in the  
above-mentioned combination.

20 The voice interval time data, though not  
specifically limited, may have two bytes. In order to  
meet the requirement of a longer voice interval,  
however, three or four bytes may be used for the voice  
interval time data.

25 [0079]

Fig. 34 is a block diagram showing an  
embodiment of a digital signal playback controller  
including the function of fast and slow playback modes

1 against the digital signal compressed in the manner  
described above.

The address counter AC is supplied with an  
address counter clock ADCK through an AND gate G3. When  
5 the voice interval data MK includes a two-byte voice  
interval mark and a two-byte voice interval time data as  
mentioned above, the read signal for the memory circuit  
RAM is outputted through four-stage shift registers SR1  
to SR4 correspondingly thereto. These shift registers  
10 SR1 to SR4 are supplied with a data shift clock DSCK  
through an AND gate G4.

The outputs A and B of the shift registers  
SR3, SR4 are inputted to a voice interval mark detector.  
The mark detector compares the bit patterns of the  
15 signals A and B to determine whether they coincide with  
the positive maximum value 01111111 and the negative  
maximum value 10000000 respectively. The detection  
signal from the voice interval mark detector is used for  
setting the flip-flops FF1 and FF2.

20 [0080]

The outputs C and D of the shift registers SR1  
and SR2 are supplied to an input A of the comparator  
CP1. The other input B of the comparator CP1 is  
supplied with the output signal of the voice interval  
25 counter. The output signal of the comparator CP1 is  
supplied through the OR gate G2 to the reset terminal R  
of the voice interval counter and the input CK of the  
repeat counter used for extending a voice interval. The

1 output Q of the repeat counter is compared with an  
extension factor N at the comparator CP2.

The output Q of the flip-flop FF is supplied  
through the inverter N2 to the OR gate G2 and the AND  
5 gates G3, G4. Upon detection of the voice interval  
mark, therefore, the operation of the address counter AC  
and the shifting operation of the shift register SR1 to  
SR4 are stopped, thereby holding the voice interval data  
in the shift registers SR1 to SR4. With the stoppage of  
10 operation of the address counter AC, the memory circuit  
RAM has the reading operation thereof suspended. The  
output signal of the comparator CP2 is supplied to the  
reset terminal R of the flip-flop FF and the repeat  
counter.

15 [0081]

The output Q of the flip-flop FF is set as a  
voice interval flag FLG and makes up a control signal  
for the AND gate G1 through the inverter N1. Upon  
detection of a voice interval mark this way, the AND  
20 gate G1 is immediately closed, thereby preventing the  
positive maximum value, the negative maximum value and  
the following time data from being outputted erroneously  
as an audio signal. Especially when the positive and  
negative maximum values are used as a voice interval  
25 mark, a large pulse-like noise would be caused if such  
values are outputted directly in their own forms.

The voice interval flag of the flip-flop FF1  
is fed back through four-stage D-type flip-flops DFF as

1 a reset signal for the flip-flop FF1. These flip-flops  
DFF, as explained below, are used to transmit the voice  
interval by the same data shift clock as the shift  
registers SR1 to SR4, thereby detecting a time period,  
5 at the end of the voice interval, in which the voice  
interval data including the voice interval mark and the  
time data thus far held in the shift-registers SR1 to  
SR4 is swept out. When it is judged by the flip-flops  
DFF that the voice interval has been ended, the flip-  
10 flop FF1 is reset.

[0082]

After the flip-flop FF2 is set upon detection  
of the voice interval mark, the reset state of the voice  
counter is cancelled through the inverter N2. The voice  
15 interval counter starts the counting operation of the  
voice interval clock SCLK in response to the cancel-  
lation of the reset state.

In normal playback mode, the N value supplied  
to the comparator CP2 is set to 1. As a result, when  
20 the count of the voice interval counter coincides with  
the voice interval time contained in the voice interval  
data, the coincidence signal outputted from the  
comparator CP1 is incremented by +1 by the repeat  
counter, thereby rendering the count as 1. Since the  
25 comparator CP2 forms a coincidence output signal at the  
same time, the repeat counter and the flip-flop FF2 are  
reset. With the resetting of the flip-flop FF2, the AND  
gates G3, G4 are opened, and the memory circuit RAM is

1 read through the address counter AC while at the same  
time restarting the shifting operation on the shift  
registers SR1 to SR4. In synchronism with the shifting  
operation of the shift registers SR1 to SR4, the voice  
5 interval flag FLG is sequentially transmitted by the  
flip-flops DFF. Specifically, until the voice interval  
data thus far held in the shift registers SR1 to SR4 is  
swept out, the flip-flop FF1 is kept in set state, and  
the resulting signal is prohibited from being outputted  
10 as an audio noise by being transmitted from the digital-  
to-analog converter DA. In synchronism with the voice  
interval data being swept out, the flip-flop FF1 is  
reset. As a result, a substantial voice interval is  
ended, and the digital audio signal outputted from the  
15 final-stage shift register SR4 is inputted to the  
digital-to-analog converter DAC through the AND gate G1,  
thereby assuring playback of an audio signal.

[0083]

In slow playback mode, the N value supplied to  
20 the comparator CP2 is set to an appropriate integer of 1  
or more. Assume that the N value is set to 2, for  
instance. When the count of the voice interval counter  
and the voice interval contained in the voice interval  
data make two rounds, the comparator CP2 forms a  
25 coincidence signal, thereby ending a voice interval of  
double length. If N is set to 3, on the other hand, the  
voice interval can be extended by a factor of three.

1 [0084]

In fast playback mode, the operation of the flip-flop FF2 is nullified. Specifically, the output signal of the voice interval mark detector is prohibited from being supplied through an AND gate or the like to the set input S of the flip-flop FF2. In such a case, the address counter AC and the shift registers SR1 to SR4 continue to be supplied with a clock, and therefore the reading operation of the memory circuit RAM is continued. Since the flip-flop FF1 is set by the detection output of the voice interval mark detector, however, the inverter N1 and the AND gate G1 prohibit the voice interval data from being inputted to the digital-to-analog converter DAC as an audio signal. Specifically, the voice interval makes up only a very short period of time during which the audio data is outputted, thereby substantially eliminating the voice interval, with the result that the fast playback is made possible as in the embodiments described above.

20 [0085]

A digital signal processor for realizing the fast and/or slow playback mode mentioned above is not only used with a player of a digital signal receiving/delivery system mentioned above but also is applicable to various reproduction systems including a digital signal processor for reproducing a digital audio signal as an analog audio signal such as the digital audio tape (DAT).

1

[0086]

Fig. 35 is a block diagram showing an embodiment of a digital-to-analog converter according to the present invention. This digital-to-analog converter, though not specifically limited, is mounted on the player used with the digital signal receiving/delivery system described above.

A well-known technique of a digital-to-analog converter is disclosed in the above-described patent publication (JP-A-61-236222). In this digital-to-analog converter, pulses of a predetermined frequency are counted repeatedly by a counter, and the output of this counter is compared with an input digital signal to be converted, so that a pulse having a width corresponding to the value of the input digital signal is outputted, and the high-frequency components are removed from the pulse output by a filter, thereby forming an analog signal.

[0087]

20

This digital-to-analog converter, which forms an output signal converted into one pulse width from an input digital signal, poses the problem that as a result of smoothing the input digital signal through a filter, a ripple component is generated making it impossible to produce an analog signal of high sound quality. Specifically, if the responsiveness (high-frequency characteristics) of an analog signal is to be improved, it is necessary to reduce the time constant of the low-



1 pass filter. If the time constant of the low-pass  
filter is thus reduced, however, the ripple component is  
undesirably increased. If the time constant of the  
filter is increased to reduce the ripple component, on  
5 the other hand, the response characteristic against the  
input signal change is deteriorated, thereby deterio-  
rating the high-frequency characteristics. Also, the  
necessity of both a counter and a comparator complicates  
the circuit configuration.

10 [0088]

The digital-to-analog converter shown in Fig.  
35 is aimed at improving such output characteristics.

The digital-to-analog converter according to  
the present embodiment includes circuits described below  
15 in order to remove the ripple component contained in the  
output signal. The input digital signal Din is supplied  
to a register. The input digital signal thus supplied  
to the register is supplied to an input A of a  
comparator. The counter is for counting pulses as a  
20 reference time signal repeatedly. The carry output  
signal CAR of this counter is supplied to a repeat  
counter. The repeat counter outputs the carry output  
CAR upon counting a designated repeat count J. This  
carry output CAR is inputted to the controller CTL for  
25 outputting a conversion-over signal EOC.

[0089]

The controller CTL, upon receiving a strobe  
synchronous with the input digital signal Din, supplies

1 a set signal S to the register thus giving an instruc-  
tion on retrieval of the digital signal Din. Though not  
specifically limited, the controller, upon retrieval of  
the input signal Din by the register in response to the  
5 reference time pulse CK of 10 MHz, supplies the same  
signal to the counter to start the counting operation.

The comparator forms a high-level output  
signal when the input digital signal Din supplied to the  
register is larger than the count Q of the counter ( $A >$   
10 B). This comparator forms a low-level signal when the  
count output Q of the counter increases beyond the data  
line input digital signal Din ( $A < B$ ). This embodiment  
including a repeat counter is such that an output pulse  
corresponding to the next input digital signal is not  
15 immediately formed as in the conventional systems but a  
pulse having a pulse width corresponding to the one  
input digital signal Din is subjected to repeated  
conversions in the number of J as designated by the  
repeat counter.

20 [0090]

Fig. 36 shows waveforms for explaining an  
example of operation of the digital-to-analog converter  
described above.

In the case where the digital input signal Din  
25 has eight bits, for instance, the period of the 10-MHz  
clock pulse CK is 0.1  $\mu$ s, and therefore when an 8-bit  
counter is used, one period is 25.6  $\mu$ s. As a result,  
when the input digital signal is a decimal 1, a high-

1 level pulse is outputted during the first 0.1  $\mu$ s and a  
low-level pulse during the remaining 25.5  $\mu$ s. When the  
input digital signal is decimal 10, on the other hand, a  
high-level signal is outputted only during the first 1  
5  $\mu$ s, and a low-level pulse during the remaining 24.6  $\mu$ s.  
In similar fashion, when the input digital signal is 100  
in decimal notation, a high-level signal is outputted  
only during the first 10  $\mu$ s, and a low-level pulse  
during the remaining 15.6  $\mu$ s. When the input digital  
10 signal assumes 255 which is the maximum decimal value, a  
high-level pulse is outputted during the first 25.5  $\mu$ s  
and a low-level pulse during the remaining 0.1  $\mu$ s.

[0091]

Fig. 36 shows a case in which the number of  
15 repetitions J is 4. When an output signal converted  
into a pulse width is outputted four times repeatedly as  
mentioned above, a conversion output signal EOC corre-  
sponding to an input digital signal Din is outputted.  
In this way, in the case of four repetitions, the  
20 conversion time for forming four pulse width modulated  
outputs within the period of fetching the data read from  
the memory circuit RAM in the player is  $25.6 \times 4 = 102.4$   
 $\mu$ s, thus making possible a conversion frequency of about  
10 kHz. This is most suitable for reproduction of a  
25 news program, a conversation, a lecture or speech. In  
reproducing a music program of high sound quality, high  
frequencies up to about 20 kHz can be reproduced in the  
process of four repetitions if the frequency of the

1 clock pulse CK is 20 MHz. If the number of repetitions  
is reduced by two while keeping the clock pulse CK at 10  
MHz, on the other hand, high frequencies up to 20 kHz  
can be reproduced in similar fashion. In this way, a  
5 combination of the frequency of the clock pulse CK and  
the number of repetitions is matched with the sampling  
period of the input digital signal.

Incidentally, when a digital signal is  
inputted again in synchronism with a strobe STB in  
10 response to the conversion output signal EOC, a  
corresponding analog-to-digital conversion is effected  
in similar manner.

[0092]

The pulse width modulated signal outputted  
15 from the comparator is smoothed by a low-pass filter  
including a resistor and a capacitor C, and is outputted  
as an analog signal Dout. According to the present  
embodiment, such pulse width modulated signals are  
outputted in a plurality of numbers. As a result, even  
20 when the response is increased by setting the time  
constant due to the resistor R and the capacitor C to a  
small value for improving the sound quality of the  
output signal, the ripple component is kept to minimum.

In the circuit according to the present  
25 embodiment which has the whole circuit capable of being  
configured of digital circuits, as compared with a case  
in which a digital circuit may be mixed with an analog  
circuit, the processes are simplified and the system may

1 be configured of a CMOS integrated circuit or the like  
which is simple in the process and low in consumption.

[0093]

Fig. 37 is a block diagram showing another  
5 embodiment of the digital-to-analog converter according  
to the present invention. The digital-to-analog  
converter according to the present embodiment is  
intended for simplifying the circuits.

According to the present embodiment, the  
10 comparator is done without and a pulse width modulated  
signal is formed corresponding to the digital signal by  
a down counter and flip-flop FF. Specifically, the down  
counter has set therein an input digital signal Din in  
synchronism with a strobe. As a result, the output  
15 signal Q of the flip-flop FF changes to high level, and  
the down counter starts counting the clock by the strobe  
mentioned above. The down counter outputs a borrow  
signal BO and resets the flip-flop FF when the count  
thereof becomes zero. This borrow signal BO is sent to  
20 the input side as conversion-over signal.

The flip-flop FF is set simultaneously with  
the starting of counting the digital signal, and is  
reset when the clock corresponding to the digital signal  
is counted. As a result, the output signal Q of the  
25 flip-flop FF is converted into a pulse width modulated  
signal corresponding to the input digital signal.

[0094]

A signal source inserted in the input side of

1 the digital-to-analog converter according to this  
embodiment outputs a digital signal and a strobe  
corresponding to a predetermined sampling period like  
the memory circuit RAM. As a result, the next digital  
5 signal is sent from the signal source not immediately  
after the conversion-over signal EOC is sent out, but on  
condition that a digital signal and a strobe are sent  
out in synchronism with the sampling period. Thus it is  
possible to produce a pulse width modulated signal  
10 corresponding to an input digital signal of a predeter-  
mined period by the setting operation synchronous with  
the strobe of the flip-flop FF and the resetting  
operation synchronous with the borrow output BO of the  
down-counter.

15 [0095]

Assume that the digital input signal Din has  
eight bits, for example. If a clock pulse CK of 10 MHz  
is used as mentioned above, the period thereof is 0.1  
 $\mu$ s, so that the maximum count is 25.5  $\mu$ s when counted by  
20 an 8-bit down counter. As a result, when the input  
digital signal is a decimal 1, the down-counter counts  
only one, and therefore a high-level pulse is outputted  
only during the first 0.1  $\mu$ s and a low-level pulse is  
outputted only during the first 0.1  $\mu$ s and a low-level  
25 pulse during the remaining 25.5  $\mu$ s until the next strobe  
is inputted. Also, when the input digital signal is a  
decimal 10, a high-level signal is outputted only during  
the first 1  $\mu$ s when ten is counted, and a low-level

1 signal during the remaining period of 24.6  $\mu$ s until a  
strobe is inputted. In similar fashion, when the input  
digital signal is decimal 100, a high-level pulse is  
outputted only during the period of 10  $\mu$ s when 100 is  
5 counted, and a low-level pulse during the remaining  
period of 15.6  $\mu$ s before the next strobe is inputted.  
When the input digital signal is 255 which is a maximum  
decimal value, on the other hand, a high-level is kept  
only during the period of 25.5  $\mu$ s corresponding to the  
10 maximum count, and a low-level pulse during the remaini-  
ng 0.1  $\mu$ s. This pulse width modulated signal is  
smoothed by a low-pass filter LPF including a resistor R  
and a capacitor C as mentioned above thereby to form an  
analog signal Vout.

15 In the case where a plurality of pulse width  
modulated signals are formed for a single input signal  
Din as in the embodiment of Fig. 35, an arrangement is  
made to generate a plurality of strobes having the  
above-mentioned period for a single input signal Din on  
20 the input side.

[0096]

Fig. 38 is a block diagram showing still  
another embodiment of a digital-to-analog converter  
according to the present invention.

25 The digital-to-analog converter shown in Fig.  
37, in which a digital signal and a strobe are required  
to be formed at regular time intervals on input side, is  
limited in applications. According to the embodiment

1 under consideration, by contrast, the period of the  
pulse width modulated signal outputted is defined by  
inserting an up-counter. Specifically, the input D of  
the up-counter is supplied with 0 and cleared by a  
5 counter load pulse LD synchronous with the strobe, while  
a down-counter is supplied with an input digital signal  
Din from the counter load pulse LD.

The down-counter and the up-counter are  
supplied with the same clock CK. The borrow output BO  
10 of the down-counter is supplied to one of the inputs of  
an AND gate G1 through an inverter N1 and the input K of  
the flip-flop FF. The clock terminal CK of the flip-  
flop FF is supplied with the above-mentioned clock  
pulse, and the input J of the flip-flop FF with the  
15 output signal of the AND gate G1. The other input of  
this AND gate G1 is supplied with a set signal generated  
from a controller GTL. The carry output CAR of the  
counter is supplied to the controller CTR.

[0097]

20 The controller CTL is turned on by a strobe ST  
received in synchronism with the digital signal Din,  
thereby outputting a counter load signal LD for the  
down-counter and the up-counter and a set signal FR for  
the flip-flop. Also, the controller CTL, in response to  
25 the clock CLK and a strobe inputted thereto, sends out a  
clock pulse to the down-counter and the up-counter, and  
upon receipt of the carry output CAR from the up-counter



1 5002, sends out a conversion-over signal EOC, thus  
entering a ready state.

The flip-flop FF is turned on at the leading  
edge of the clock pulse. In the process, the flip-flop  
5 FF is held if the inputs J and K are 00 (both low in  
level), reset if the inputs J and K are 01 (low and high  
in level), set if the inputs J and K are 10 (high and  
low in level), and inverted if the inputs J and K are 11  
(both high in level).

10 [0098]

Now, the operation of the digital-to-analog  
conversion will be described in detail.

In initial state, all the counters and the  
flip-flop FF are reset. When a conversion start signal  
15 is inputted to the strobe input terminal ST of the  
controller CTL, the controller CTL sets the output  
signal from the conversion-over signal terminal EOC to  
logic "1" and thus declares that conversion is going on.

The controller CTL outputs a count load signal  
20 LD, thereby loading the down-counter with an input  
digital signal, and the up-counter with 0 in synchronism  
with the leading edge of the clock CK. The down-counter  
and the up-counter start the counting operation at the  
end of loading.

25 The controller CTL outputs a set signal FR of  
the flip-flop FF at a point later than the counter load  
signal LD by one half period of the counter clock.  
Since the borrow output BO of the down counter is logic

1 "0", the flip-flop FF has the input J thereof in "1" state and the input K in "0" state, and is thus set in synchronism with the leading edge of the clock pulse.

[0099]

5 The down counter performs the down-counting operation (-1) each time of arrival of the clock, and when the count becomes 0, outputs the borrow output BO. As a result, the borrow signal BO changes to logic "1", and the input J of the flip-flop FF to "0", and the  
10 input K thereof to "1". Thus the flip-flop FF is reset in synchronism with the leading edge of the clock pulse.

When the input digital signal Din is decimal 0, the borrow output BO of the down-counter and the set signal FR of the controller CTL are outputted in the  
15 same timing. According to the present embodiment including an AND gate G1 to give priority to the borrow output BO of the down-counter. This AND gate G inhibits the set signal FR of the flip-flop FF from the controller CTL. In this way, when the digital signal Din is  
20 decimal 0, no pulse is outputted from the flip-flop FF. When the digital signal Din is 1 or more, in contrast, a pulse having a pulse width corresponding to the output Q of the flip-flop FF is outputted. The output signal thus subjected to pulse width modulation is smoothed by  
25 a low-pass filter LPF thereby to form an analog signal Vout.

[0100]

The up-counter continues the counting

1 operation, and outputs a carry signal CAR when the count  
reaches the maximum. The controller CTL, upon receipt  
of the carry signal CAR, changes the conversion-over  
signal EOC to logic "0" thereby to end the whole series  
5 of the converting operation. Upon completion of the  
conversion, the next digital signal is inputted.  
Specifically, in the case where the up-counter is  
provided as described above, an address signal is  
generated by the conversion-over signal EOC following a  
10 digital-to-analog conversion to read the next input  
digital signal.

As explained above, when the input digital  
signal Din and the strobe are inputted, the above-  
mentioned operation is repeated to form an analog signal  
15 Vout corresponding to the input digital signal Din. The  
controller CTL raises the conversion-over signal EOC to  
high level and notices the fact to an external circuit  
during the conversion process, and continues the  
conversion without answering to a strobe ignoring the  
20 notice.

In reducing the ripple component of the analog  
conversion output Vout, a repeat counter or the like is  
provided for each conversion start signal like a strobe  
to repeat a designated number of digital-to-analog  
25 conversions as mentioned above. In the case where no  
input of a digital signal Din is assured during this  
repetition, a register should be provided to fetch an

1 input digital signal in the same manner as described above.

The embodiments explained with reference to Figs. 35 to 38 may be applied widely as a signal  
5 converter for converting a digital signal into a pulse width modulated signal as well as to a digital-to-analog converter.

[0101]

Fig. 39 is a basic block diagram showing an  
10 embodiment of a switch input circuit for the player used with the digital receiving/delivery system described above.

As described already, the player is reduced in size and thickness so as to be compatible with an IC  
15 memory card or the like. As a result, it is considered important to reduce the switches or the like for designating an operation mode. In view of this, according to this embodiment, signals 3-1 to 3-n for designating the states 1 to n are formed by a state controller 2  
20 receiving an on/off signal of a key switch 1. By doing so, a package of switches 1 can be accommodated in a limited space of the small and thin player as described above.

[0102]

25 Fig. 40 is a block diagram for explaining an embodiment of a specific configuration of a state controller.

1           According to this embodiment, an on time of  
the switch 1 is judged by the state controller 2. The  
state controller 2 forms a signal 13-1 for turning on  
state A unconditionally once the switch is turned on  
5 regardless of the on time T of the switch 1. The state  
controller 2 forms a signal 13-2 for turning on state B  
when the on time T of the switch 1 is smaller than a  
predetermined time length M ( $M > T$ ). The state  
controller 2 further forms a signal 13-3 for turning on  
10 state C when the on time T of the switch 1 is judged to  
be larger than a predetermined time length M ( $M \leq T$ ).  
By combining the signals 13-1 to 13-3 representing these  
three states A to C, the playback control operation  
mentioned below is realized.

15           [0103]

Fig. 41 is a schematic diagram for explaining  
this operating mode.

The player is set in a stop state 4 immediate-  
ly after power is thrown in. In this state 4, assume  
20 that the switch is turned on. A signal 1a indicating an  
unconditional state A regardless of the on time T is  
formed to set the player in playback state 5. In this  
playback state 5, it is necessary to select one of two  
choices, one to change to a pause state 6 and the other  
25 to return to the stop state 4. When the switch is  
turned on again, the signal indicating the state A is  
formed and the time judgement 7 is started, thereby  
judging the time T turned on. If the judgement is a

1 signal 1c indicating the state B, the player is set to  
the pause 6. If the judgement is a signal 1e indicating  
the state C, on the other hand, the player is returned  
to the stop state 4. In the stop state 6, the only  
5 meaningful operation is to return to the playback state  
4, and therefore the switch is only turned on so that  
the playback state 5 is restored by the signal 1d  
indicating the state A as described above.

[0104]

10 In the case where a plurality of types of  
operation are designated by a switch, the disadvantage  
is a complicated operating procedure. According to the  
embodiment under consideration, in order to enable the  
user to master the operating procedure easily, light-  
15 emitting diodes or liquid crystal display devices are  
provided as elements corresponding to the stop state 4,  
playback state 5 and the pause state 6 shown in Fig. 39.  
These elements are lit in accordance with the present  
state, and are combined with arrows shown in Fig. 39  
20 thereby to indicate a state into which a change is  
possible by the input of the states A to C. This  
indication is effected only for a predetermined time of  
switching operation to save power consumption in the  
case where a light-emitting diode is used as the display  
25 unit.

[0105]

Fig. 42 is a block diagram showing another  
embodiment for explaining a specific configuration of a

1 state controller.

According to this embodiment, the number of turnings on of the switch 1, not the on time T of the switch 1 as mentioned above, is judged by the state controller 2. The state controller 2 counts the number of turnings on of the switch 1 and forms a signal 23-1 for entering state A if the number of turning on is one. When the number of turnings on of the switch 1 is two, on the other hand, a signal 13-2 for entering state B is formed. By combining the signals 23-1 and 23-2 indicating two states A and B in this way, the playback control operation mentioned below is realized.

[10106]

Fig. 543 is a schematic diagram for explaining the operating mode.

Immediately after power is switched on, the player is set to the stop state 4 as described above. When the switch is turned on once under this state 4, a signal 2a indicating the state A is formed to set the player to playback state 5. In this playback state 5, it is necessary to select one of the two choices, one for changing to the pause state 6 and the other for returning to the stop state 4. When the switch is turned on once, the signal 2n indicating the state A is formed to set the player to the pause state 6. As an alternative, if the switch is turned on twice, the signal 2e indicating the state B is formed to return the player to the stop state 4. In this embodiment, the

1 stop state 4, as well as the playback state 5, may be  
restored from the pause state 6. As a result, if the  
switch is turned on once in the pause state 6, a signal  
2c indicating the state A is formed to shift the player  
5 to the playback state 5. When the switch is turned on  
twice in the pause state 6, a signal 2d indicating the  
state B is formed to shift the player to the stop state  
4. According to this embodiment, too, the operating  
procedure is easily mastered by plotting corresponding  
10 display units and arrows in Fig. 41 as in the preceding  
embodiment.

[0107]

Fig. 44 is a schematic diagram showing an  
embodiment of a storage area management system of the  
15 memory circuit RAM of the player.

In order to assure efficient use of the  
storage capacity of the memory circuit RAM mounted in  
the player against a plurality of pieces of information,  
the memory circuit RAM is divided into a contents area  
20 and a data area. The contents area, though not speci-  
fically limited, has four contents PA0 to PA3, capable  
of storing block addresses BA0 to BA3 respectively. The  
contents PA0 to PA3 are selected by program select sig-  
nals PSL1, PSL2 and the like thereby making it possible  
25 to write or read the block addresses BA0, BA1, etc.

In the above-described digital receiving/  
delivery system, the server, when connected with the  
player, accesses the contents area and reads an



1 effective block address. As a result, the server is in  
a position to know a vacant area of the memory circuit  
RAM of the player. When a new digital signal to be  
received is designated, the block address is stored in  
5 the vacant contents area while at the same time storing  
a digital signal in the vacant area.

[0108]

If the contents are in short supply or the  
vacant storage capacity is lacking for the digital  
10 signal received, a digital signal that has been already  
stored and that may be erased by display is selected,  
and by erasing the particular digital signal, a new  
digital signal is inputted. In the process, the digital  
signal that is already stored in the player is also read  
15 out, and an address is allocated in such a manner as not  
to cause any vacancy of storage area in accordance with  
the storage capacity of the new digital signal.

[0109]

In Fig. 44, the contents PA0 are addressed by  
20 a program select signal PSL1, so that the block address  
BA0 stored therein is read and set in the address  
counter. Assuming that the block address BA0 set in the  
address counter is the data block of the head address of  
the data area as shown by solid line, for example, the  
25 ID code at the head of the block and subsequent  
addresses start to be read sequentially. The last  
address of the data, though not specifically specified,  
has an end mark END stored therein, by detection of

1 which the reading process is ended. In this configura-  
tion, it is sufficient to store only the head address in  
the contents and therefore the address information can  
be reduced.

5 [0110]

Also, the contents PA2 are accessed by the  
program select signal PSL2, and the block address BA2  
stored therein is read and set in the address counter.  
In the case where the block address set in the address  
10 counter makes up an intermediate block as shown by  
dotted line, for instance, the addresses having the head  
ID code of the particular block and subsequent addresses  
start to be read in that order. The last address of the  
data has the end mark END stored therein in the manner  
15 similar to the preceding case, and the reading process  
is ended upon detection of the end mark END.

[0111]

Assume that some data blocks storing the  
above-mentioned two types of program are vacated by  
20 erasure of a digital signal corresponding to the  
contents PA1 or otherwise, for example. The server  
changes the block address BA2 of the contents PA2 to an  
address of the end mark END of the data area corre-  
sponding to the contents PA0, while at the same time  
25 writing a corresponding digital signal. By doing so, a  
digital signal corresponding to the program newly  
received is usable successively for the remaining vacant  
areas.

1           The player may be connected with the server so  
that the contents area and the data area may be cleared  
and a new digital signal may be stored. In such a case,  
desired programs may be reserved by designating a no-  
5 erasure on the player side or a no-erasure program as an  
operation of receiving of a digital signal with the  
server.

[0112]

Fig. 45 is a schematic diagram showing another  
10 embodiment of the storage area management system of the  
memory circuit RAM of the player.

According to this embodiment, a digital signal  
is stored and managed by a contents memory and a data  
memory. The contents memory can store a maximum of four  
15 types of digital signals (programs) including contents 1  
to 4, for example. The contents memory may store only  
the head address as in the aforementioned embodiment or  
the contents information in addition to the end address  
or ID code. This contents information, though not  
20 specifically limited, includes character information, so  
that the program contents can be displayed by characters  
with a liquid display unit mounted in the player.

Each content of the contents memory and the  
data area of the data memory is arranged as desired in  
25 such forms as data 2, data 1, data 4 and data 3, for ex-  
ample, from the head address side of the data memory in  
the order of storage. Specifically, digital signals are  
stored in the data memory in the order of designation.

1 [0113]

Fig. 44 is a block diagram showing the essential parts of an embodiment of the player with the contents function added thereto.

5 The controller CTL includes a switch SW1 for designating contents (designating programs) in addition to the switch SW2 for operation control mentioned above. When this switch SW1 is turned on, though not specifically limited, a +1 pulse is supplied to the contents  
10 address counter (AC), and the contents memory is accessed. The contents information read out of the contents memory is stored in the contents register whereby such characters as title are displayed on the liquid crystal display LCD.

15 [0114]

The head address read out of the contents memory is set in the address counter AC of the data memory, while the end address and the ID code are loaded in the registers RED respectively. The ID code is  
20 transmitted to the controller CTL is decoded for automatically setting the sampling frequency, the data length, the stereo/monaural mode and the like.

The address signal outputted from the address counter AC is used for accessing the data memory on the  
25 one hand and is supplied to the comparator CP on the other hand. The other input of the comparator CP is supplied with the last address loaded in the register REG. As a result, when a digital signal (data)

1 corresponding to the designated contents is completely  
read, this fact is detected by the comparator CP and an  
end signal is inputted to the controller CTL, thereby  
ending the operation of reading a series of digital  
5 signals.

[0115]

In the above-mentioned indexing function, the  
number of contents may be four or as desired. If such a  
number is the Nth power of 2, however, a binary address  
10 counter can be conveniently used directly and selection  
is facilitated. Also, in the case where the contents  
memory is provided separate from the data memory, they  
are accessible in parallel independently of each other  
thereby to simplify the control of the address counter.  
15 The contents memory, as in the embodiment of Fig. 44,  
may be course be configured by the use of a predeter-  
mined storage area of the data memory.

[0116]

The effects obtained from the embodiments  
20 described above are as follows:

(1) In receiving/delivering a digital signal, a  
player is electrically connected one-to-one with a  
digital signal source, so that a specified digital  
signal is received and stored in a memory in the form of  
25 electrical signal and the digital signal stored  
independently in the memory is reproduced. In this  
configuration, the player receives the digital signal  
and reproduces it independently in the form of

1 electrical signal, so that the value of the digital  
signal delivered is exhibited in direct form.

(2) As a result of the effect described in (1)  
above, the digital signal delivered as a commodity or  
5 the like may remain in the form of electrical signal and  
therefore can be easily processed or produced or the  
selling system thereof easily set up.

(3) As a result of the effect described in (1)  
above, the value of the digital signal itself received/  
10 delivered is recognized as a commodity or the like, and  
the player has a simple function of reproducing the  
particular value. The player thus has a simple  
configuration and is easily operated by any one.

(4) A digital signal is received from a digital  
15 signal source by a terminal device through a communica-  
tion channel or an appropriate storage medium. A player  
and a connector are electrically connected with the  
terminal device to receive/deliver a digital signal,  
whereby a digital signal selling system is provided for  
20 selling a digital signal as a commodity or the like both  
rationally and at high speed.

[0117]

(5) A magnetic disk memory having a comparatively  
large storage capacity is used as a backup memory for  
25 the terminal device, and the digital signal large in the  
amount of receiving/delivery or updated with time is  
stored in a buffer memory configured of a semiconductor

1 memory accessible at high speed, thus realizing an  
efficient receiving/delivery of a digital signal.

(6) The terminal device is provided with the  
microcomputer function to manage the magnetic disk  
5 memory or the buffer memory and to exchange a digital  
signal with the source through a communication channel.  
Also, the storage area of the memory in the player is  
managed to permit effective utilization of the memory as  
well as simplification of the player.

10 (7) The terminal device is provided with the  
function of monitoring a part of the digital signal for  
a predetermined length of time, thereby preventing a  
selection error or facilitating the selection of an  
intended digital signal.

15 (8) The digital signal received/delivered is  
limited to audio information as a digital audio signal,  
and therefore the player function is simplified to  
storage and playback.

[0118]

20 (9) The digital signal received/delivered has  
added thereto an ID code, whereby the playback  
conditions for the player are automatically designated  
thereby to receive/deliver a variety of digital signals  
corresponding to a given information program while at  
25 the same time offering an operating ease.

(10) By providing a card-like memory section  
replaceable from the player body, various RAM, EEPROM or

1 ROM may be used as a memory, thereby increasing the  
variety of functions.

(11) The outline of the player and the connector  
are compatible with the existing memory card, whereby an  
5 internal memory can be used equivalently to the existing  
memory card.

(12) As a result of the effects described in (10)  
and (11) above, the multiple functions and enlarged  
applications of the player are assured.

10 (13) The player is provided with a security func-  
tion for protecting the input and/or output operation of  
the memory in accordance with a password or a password  
coincidence detection signal, whereby easy duplication,  
eavesdropping or the like is prevented thereby increas-  
15 ing the commercial value of a digital signal received/  
delivered.

(14) As a part of the memory section of the player,  
a thin card-like memory is replaceably mounted. This  
makes it possible to enlarge the storage capacity or  
20 reproduce a program configured of various ROMs as  
required, thereby realizing a variety of functions.

[0119]

(15) The security system may be configured in such  
a manner that at least one bit of digital signal at the  
25 address input section or the data input and/or data  
output of the digital signal memory circuit is inverted,  
or is replaced by another bit, thereby realizing a  
confidentiality with a simple configuration.



1 (16) The player is provided with a storage area or  
a contents memory for storing contents information  
including a storage address corresponding to a plurality  
of digital signals, and a data area or a data memory  
5 accessible by the storage address, so that a digital  
signal as a plurality of types of information is  
efficiently stored in the memory.

(17) The operation of the player is controlled by  
designating a plurality of types of operating modes by a  
10 combination of on time or the number of turnings on, of  
a key switch thereby realizing a miniaturization and  
reduced thickness of the player.

[0120]

(18) The voice interval of a digitized audio signal  
15 is detected, and the digital signal inputted to a  
digital-to-analog converter is forcibly replaced by a  
signal corresponding to an AC-like 0 level during the  
particular voice interval, thereby eliminating a  
cacophonous quantizing noise.

20 (19) A voice interval is detected on the basis of  
output signals of a pair of comparators for comparing a  
digital signal corresponding to adjustable positive and  
negative levels considered voiceless with a reproduced  
digital signal, thereby making it possible to detect a  
25 voice interval accurately in accordance with the  
contents of a program of a digital signal.

(20) The voice interval of a digitized audio signal  
is detected and the length thereof is extended or

1 enlarged thereby to permit a slow playback with high  
sound quality.

(21) The operation of updating the address of a  
memory having a digital signal stored therein is delayed  
5 substantially behind normal operation by a simple  
configuration, thereby realizing a slow playback with  
high sound quality.

[0121]

(22) The voice interval of a digitized audio signal  
10 is detected, and by shortening the length thereof, a  
fast playback is made possible while maintaining a high  
sound quality.

(23) The operation of updating the address of a  
memory having a digital signal stored therein is  
15 increased in speed as compared with normal operation by  
a simple configuration, thereby realizing a fast  
playback while maintaining a high sound quality.

(24) By replacing a voice interval of a digital  
signal with a voice interval code data and voice  
20 interval time data, data compression is made possible,  
while at the same time producing a voice interval  
corresponding to the time data. Further, by adding a  
simple circuit, the time data is enlarged with a longer  
voice interval or neglected for playback, thus permit-  
25 ting fast or slow playback.

(25) At least two continuous digital signals corre-  
sponding to substantially positive and negative maximum  
values are combined as a voice interval code, whereby

1 the digital audio signal and the voice interval code are discriminated easily.

(26) A maximum voice interval is set and the voice interval enlarged with the slow playback is limited not  
5 to exceed the maximum voice interval, whereby the wasteful time required for playback in slow playback mode is eliminated.

[0122]

(27) A digital input signal is stored in a memory,  
10 and the output of a counter for performing the counting operation corresponding to the maximum value of the digital input signal in response to a reference time pulse is compared with the digital signal stored in the memory thereby to form a pulse width modulated signal.  
15 This operation is repeated a plurality of times by a repeat counter, thereby producing an analog signal of high sound quality.

(28) A digital signal supplied in a predetermined period corresponding to the maximum value of the digital  
20 signal is inputted to a down counter to form a reference time pulse by a simple circuit, thereby producing a pulse width modulated signal corresponding to the digital signal.

(29) A predetermined period corresponding to the  
25 maximum value of the digital signal is formed by an up counter for performing the counting operation corresponding to the digital input signal in response to the reference time pulse, whereby a digital signal corre-

1 sponding to the address conversion can be inputted with  
a simple configuration.

[0123]

5 The present invention which has been explained  
above with reference to embodiments is not limited to  
such embodiments and various modifications are of course  
possible without departing from the spirit of the  
invention. In a digital signal receiving/delivery  
system, for example, a digital signal may be not only  
10 sold as a commodity but also offered free of charge to a  
person specified by the player as one of the services  
offered by securities firms, financial institutions or  
the like. As an alternative, the whole digital signal  
may be utilized for receiving/delivery of information  
15 required periodically or from time to time by a  
collective agreement. Also, the digital signal may be  
in such a form as capable of being transmitted by an  
audio signal like the data required for language study  
or memorization for various test objects.

20 Further, a digital signal receiving/delivery  
system mentioned above makes it possible to build a very  
efficient and timely futuristic media for supplying  
various information and amenities using a digital audio  
signal in place of the conventional newspaper, weekly  
25 magazines, etc. using prints.

[0124]

The player may be constructed of a connector  
connectable with an extending ROM card or RAM card. In

1 such a case, in order to prevent the player itself from  
being increased in thickness, the ROM or RAM card is be  
desirably made up of a thin plastic card with a memory  
chip built therein. The ROM card is convenient for a  
5 music program or language learning. The RAM card makes  
up effective means for enlarging the memory capacity.  
The RAM card is effective, for example, when receiving a  
music program or the like with a long performance time.

[0125]

10 The configuration, function, etc. of the  
terminal device and the player used with the digital  
signal receiving/delivery system may take various forms  
of embodiment. The memory built in the player may be a  
static RAM or a combination of a dynamic RAM and an  
15 automatic refresh circuit as well as a pseudo-static RAM  
mentioned above, or as a further alternative, may be a  
flash memory (EEPROM) or any of various ROMs or a small,  
thin rewritable optical disk.

The digital signal may be character or image  
20 information, or a combination of an audio signal and a  
character or image information as well as an audio  
signal mentioned above. For reproducing such character  
or audio information, a display unit is required. A  
display unit, though not specifically limited, may  
25 include a thin and lightweight liquid crystal display  
unit.

1

[0126]

[Effect of the Invention]

Representative effects obtained from the present invention disclosed in this application will be explained. Specifically, in receiving/delivery of a digital signal, a player as a terminal unit corresponding one-to-one to a digital signal source is electrically connected, a specified digital signal is received in the form of electrical signal and stored in a memory, and a digital signal stored independently by the player is reproduced. In this system, the player receives a digital signal in the form of electrical signal and reproduces it independently, and therefore the value of the digital signal received/delivered can be exhibited as it is. And, since the receiving/delviery is in the form of digital signal, the processing, manufacturing or sales system thereof is easily constructed. At the same time, since the player is simple in configuration and easy to operate, any one can handle it. Also, by detecting a voice interval of a digitized audio signal and enlarging or shortening the voice interval, the slow or fast playback is realized while maintaining a high sound quality. Also, the signal of a pulse width corresponding to a digital input signal is repeated a plurality of times, whereby it is possible to reduce the ripple at the time of smoothing, thus making it possible to obtain a hgh-quality analog signal.

1 [Brief Description of Drawings]

[Fig. 1]

A block diagram showing the essential parts of  
a digital signal receiving/delivery system according to  
5 an embodiment of the present invention.

[Fig. 2]

A block diagram showing an input section of  
the terminal device of Fig. 1.

[Fig. 3]

10 A block diagram showing a memory section of  
the terminal device of Fig. 1.

[Fig. 4]

A block diagram showing an output section of  
the terminal device of Fig. 1.

15 [Fig. 5]

A block diagram showing an embodiment of the  
player used with a digital signal receiving/delivery  
system according to the present invention.

[Fig. 6]

20 A plan view showing an embodiment of a package  
board configuring the player.

[Fig. 7]

A side view showing an embodiment of a package  
board accommodated in a case.

25 [Fig. 8]

A plan view showing another embodiment of the  
player.

[Fig. 9]

1           A block diagram showing an embodiment of the  
player body and the memory section of Fig. 8.

[Fig. 10]

5           A block diagram showing an embodiment of a  
power supply system of the player.

[Fig. 11]

          A diagram showing the configuration of an  
embodiment of the digital signal transferred from a  
terminal device to the player.

10           [Fig. 12]

          A block diagram showing an embodiment of the  
player corresponding to the digital signal with the ID  
signal of Fig. 11 inserted therein.

[Fig. 13]

15           A circuit diagram showing an embodiment of a  
quantizing noise remover according to the present  
invention.

[Fig. 14]

20           A diagram showing waveforms for explaining an  
example of the operation of the quantizing noise remover  
of Fig. 13.

[Fig. 15]

25           A circuit diagram showing an embodiment of a  
security circuit used in a digital signal selling system  
according to the present invention.

[Fig. 16]

          A circuit diagram showing another embodiment  
of the security circuit used in a digital signal selling



1 system according to the present invention.

[Fig. 17]

A circuit diagram showing still another  
embodiment of the security circuit used with a digital  
5 signal selling system according to the present  
invention.

[Fig. 18]

A circuit diagram showing a further embodiment  
of the security circuit used in a digital signal selling  
10 system according to the present invention.

[Fig. 19]

A circuit diagram showing a still further  
embodiment of the security circuit used in a digital  
signal selling system according to the present  
15 invention.

[Fig. 20]

A specific circuit diagram showing an  
embodiment of a bit exchanger used in the security  
circuit of Fig. 20.

20 [Fig. 21]

A block diagram showing an embodiment of a  
digital audio signal processor for realizing the fast  
and slow playback according to the present invention.

[Fig. 22]

25 A block diagram showing a specific example of  
a fast playback circuit according to the present  
invention.

1 [Fig. 23]

A block diagram showing a specific example of the slow playback circuit according to the present invention.

5 [Fig. 24]

A diagram showing waveforms for operation corresponding to the fast playback circuit of Fig. 22.

[Fig. 25]

A diagram showing waveforms for operation  
10 corresponding to the slow playback circuit of Fig. 23.

[Fig. 26]

A block diagram showing another embodiment of the fast playback circuit according to the present invention.

15 [Fig. 27]

A block diagram showing another embodiment of a slow playback circuit according to the present invention.

[Fig. 28]

20 A diagram specifically showing another embodiment of the slow playback circuit according to the present invention.

[Fig. 29]

A schematic diagram for explaining an example  
25 of operation of the slow playback circuit shown in Fig. 28.

[Fig. 30]

A schematic diagram for explaining another

1 example of operation of the slow playback circuit shown  
in Fig. 28.

[Fig. 31]

A schematic diagram for explaining still  
5 another example of operation of the slow playback  
circuit shown in Fig. 28.

[Fig. 32]

A waveforms for explaining another embodiment  
of the fast and slow playback operations according to  
10 the present invention.

[Fig. 33]

A bit pattern diagram showing an embodiment of  
a voice interval signal MK in Fig. 32.

[Fig. 34]

15 A block diagram showing an embodiment of a  
digital signal playback circuit including the fast/slow  
playback mode for a digital signal representing a  
compressed data.

Fig. 35A block diagram showing an embodiment  
20 of a digital-to-analog converter according to the  
present invention.

[Fig. 36]

A waveform diagram for explaining an example  
of operation of the digital-to-analog converter of Fig.  
25 35.

[Fig. 37]

A block diagram showing another embodiment of  
a digital-to-analog converter according to the present

1 invention.

[Fig. 38]

A block diagram showing still another  
embodiment of a digital-to-analog converter according to  
5 the present invention.

[Fig. 39]

A fundamental block diagram showing an  
embodiment of a switch input circuit of a player used in  
a digital signal receiving/delivery system.

10 [Fig. 40]

A block showing a specific configuration of a  
state controller according to an embodiment of the  
present invention.

[Fig. 41]

15 A schematic diagram for explaining the  
operating mode of the embodiment shown in Fig. 40.

[Fig. 42]

A block showing a specific configuration of a  
state controller according to another embodiment of the  
20 invention.

[Fig. 43]

A schematic diagram for explaining the operat-  
ing mode according to the embodiment shown in Fig. 42.

[Fig. 44]

25 A schematic diagram showing an embodiment of a  
storage area management system for a memory RAM built in  
the player.

1 [Fig. 45]

A schematic diagram showing another embodiment of a storage area management system for a memory RAM built in the player.

5 [Fig. 46]

A block diagram showing the essential parts of an embodiment of the player with an indexing function of Fig. 45 added.

[Designation of Reference Characters and Numerals]

LPF ... Low-pass filter, MPX ... Multiplexer, S/H ... Sample & hold circuit, ADC ... Analog/digital converter, INCT ... Input section controller, NIF ... Network interface, CPU ... Microprocessor, ROM ... Read-only memory, RAM ... Random access memory (memory), HDDC ... Hard disk controller, LCDC ... LCD controller, VMEINF ... VME bus interface, HDD ... Hard disk memory, LCD ... Liquid crystal display, OUTINF ... Output interface, PCTL ... Player controller, BM ... Buffer memory, MOCTL ... Monitor controller, MONT ... Monitor, P/S ... Parallel/serial converter, AC ... Address counter, CTP ... Controller, LSI ... Large scale integration (gate array), DAC ... Digital/analog converter, AMP, AMP1, AMP2 ... Amplifier, BAT ... Power supply, S2 to S3 ... Power switch, E1 to E3 ... Battery, SEL ... Selector, REG ... Register, OSC ... Oscillator, CPG ... Clock generator, CP, CP1 to CP3 ... Comparator, EOR ... Exclusive OR gate, G, G1 to G4 ... Gate, N, N1

to N3 ... Inverter, AU ... Adder, MU ... Multiplier, FF,  
FF1 to FF2 ... Flip-flop, MK ... Voice interval signal,  
SR1 to SR4 ... Shift register, DFF ... D-type flip-flop.

1 ... Key switch, 2 ... Operating condition  
controller, 3 ... Signal (operating condition), 4 ...  
Stop state, 5 ... Playback state, 6 ... Pause, 7 ...  
Time judge state.

1 [Title of Document]      Abstract

[Summary]

[Object]    There is provided a digital signal receiving/  
delivery system realizing the sale of information and  
5 the like having a commodity value in the form of  
electrical digital signal, and a digital audio signal  
processor and a signal processor suitable therefor.

[Structure]    In receiving/delivery of a digital  
signal, a digital signal source is connectd electrically  
10 with a player as a terminal unit corresponding one-to-one  
to the digital signal source, a specified digital signal  
is received in the form of electrical signal and stored  
in a memory, and the digital signal stored is reproduced  
independently by the player. A voice interval of a  
15 digitized audio signal is detected and enlarged to  
realize slow playback, while the voice interval is  
shortened to realize fast playback. A signal of a pulse  
width corresponding to a digital input signal is  
repeated a plurality of times in a single signal  
20 conversion period.

[Effect]    The player receives a digital signal in the  
form of electrical signal and reproduces it independent-  
ly. Therefore, the value of the digital signal  
received/delivered can be exhibited in its direct form.  
25 Thus the processing, manufacturing and sales systems  
thereof can be easily constructed. Also, since the  
player is simple in configuration and easy to operate,  
it can be handled by any one. By enlarging or

- 1 expanding the voice interval of a digital audio signal substantially, the fast or slow playback becomes possible without deteriorating the sound quality. And, by forming a repetitive pulse width modulation signal
- 5 corresponding to a digital input signal, the ripple caused at the time of smoothing can be greatly reduced, thus producing a high-quality analog signal.

[Selected Drawing]      Fig. 5

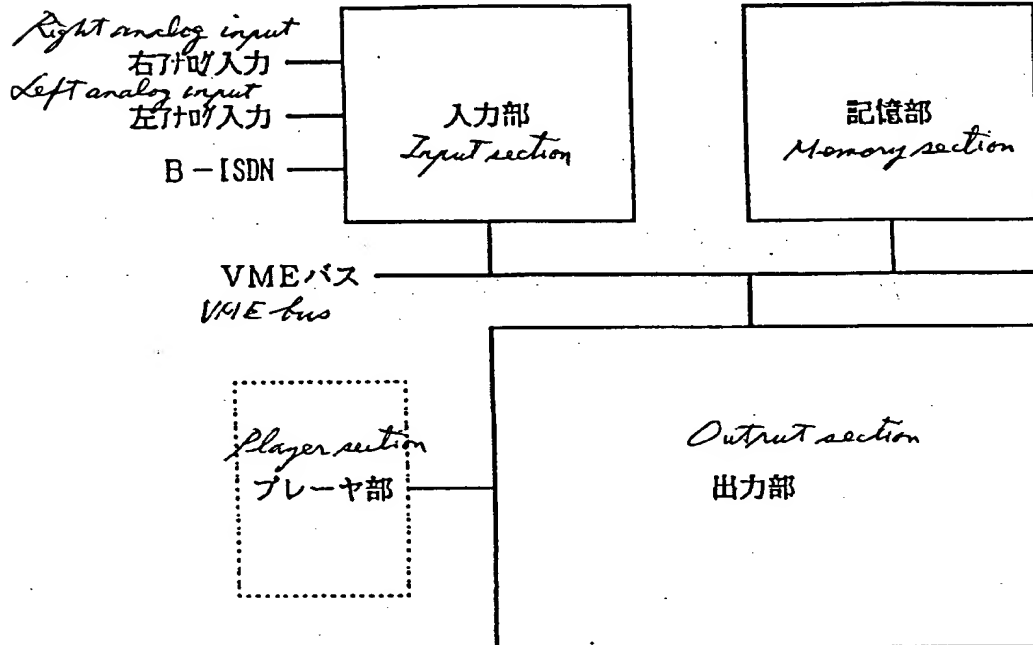


~~Document name~~ [Title of Document]

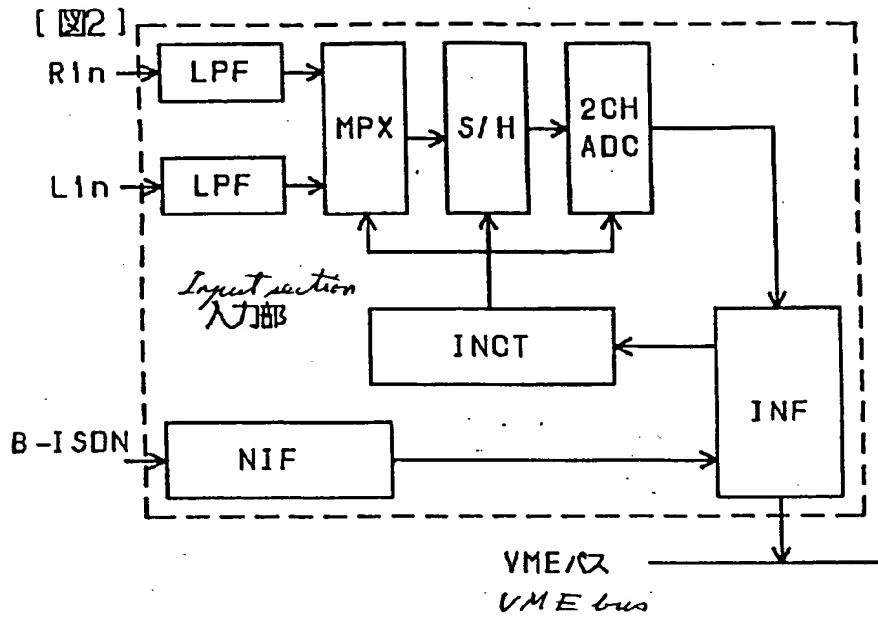
【書類名】 図面その1 Drawing NO.1

【図1】 [Fig.1]

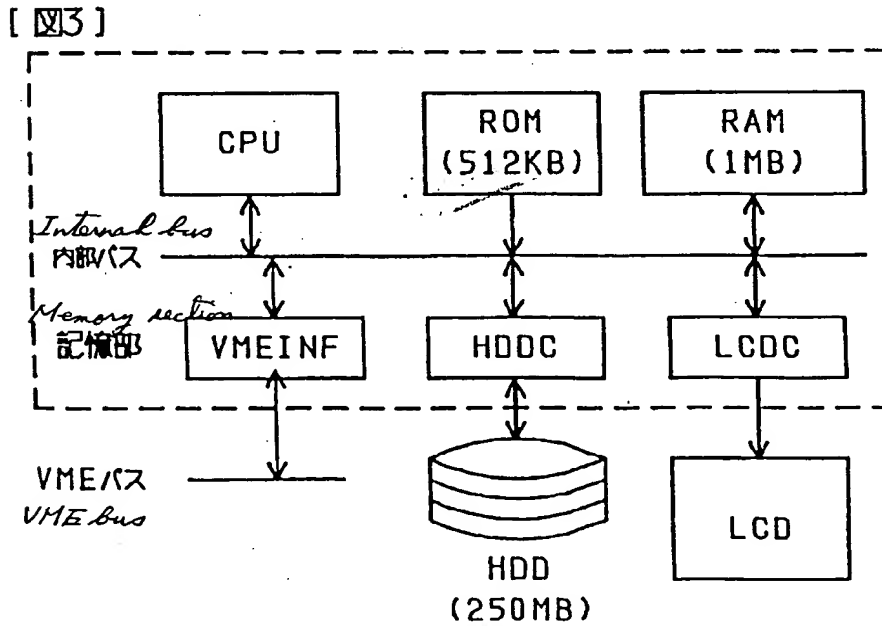
(図1) [Fig.1]



【図2】  
[Fig. 2]



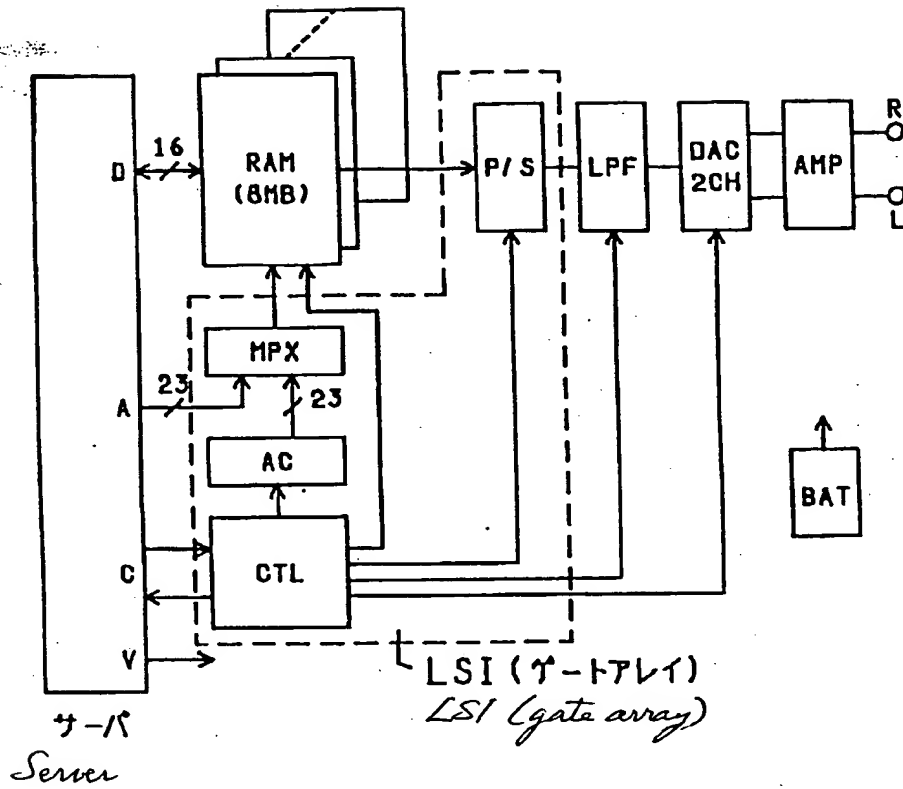
【図3】  
[Fig. 3]



【図5】

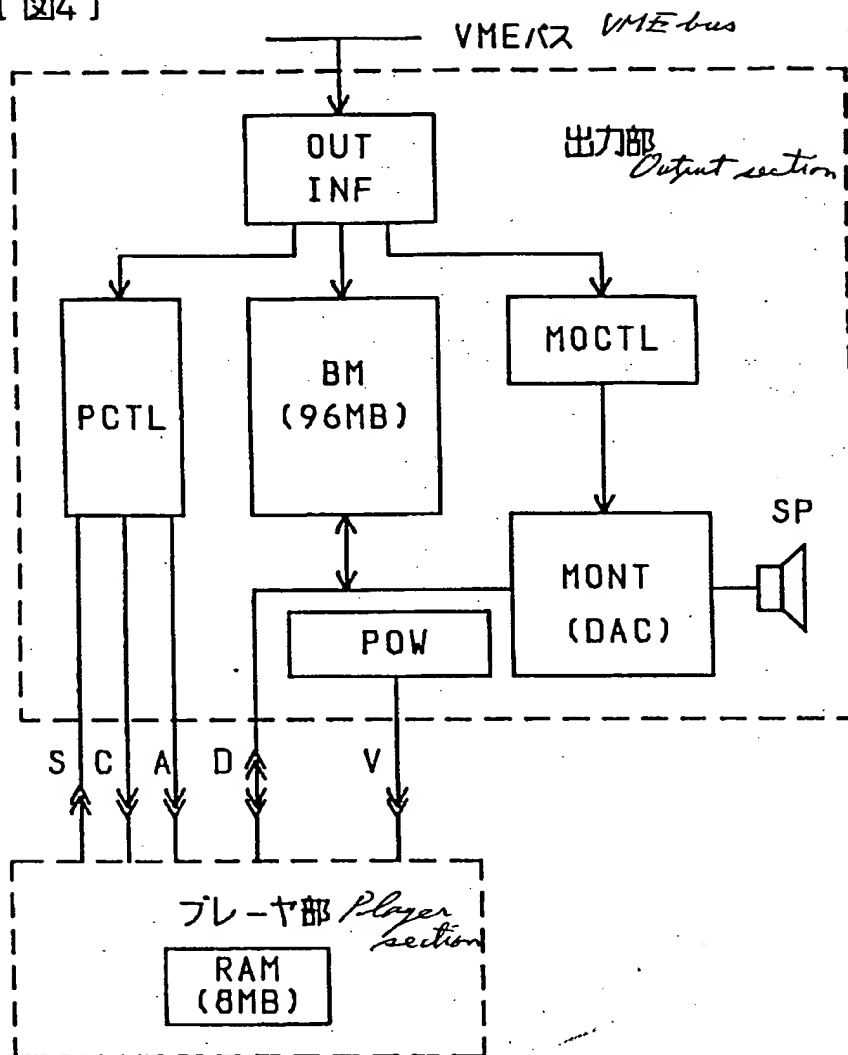
[Fig.5]

【図5】



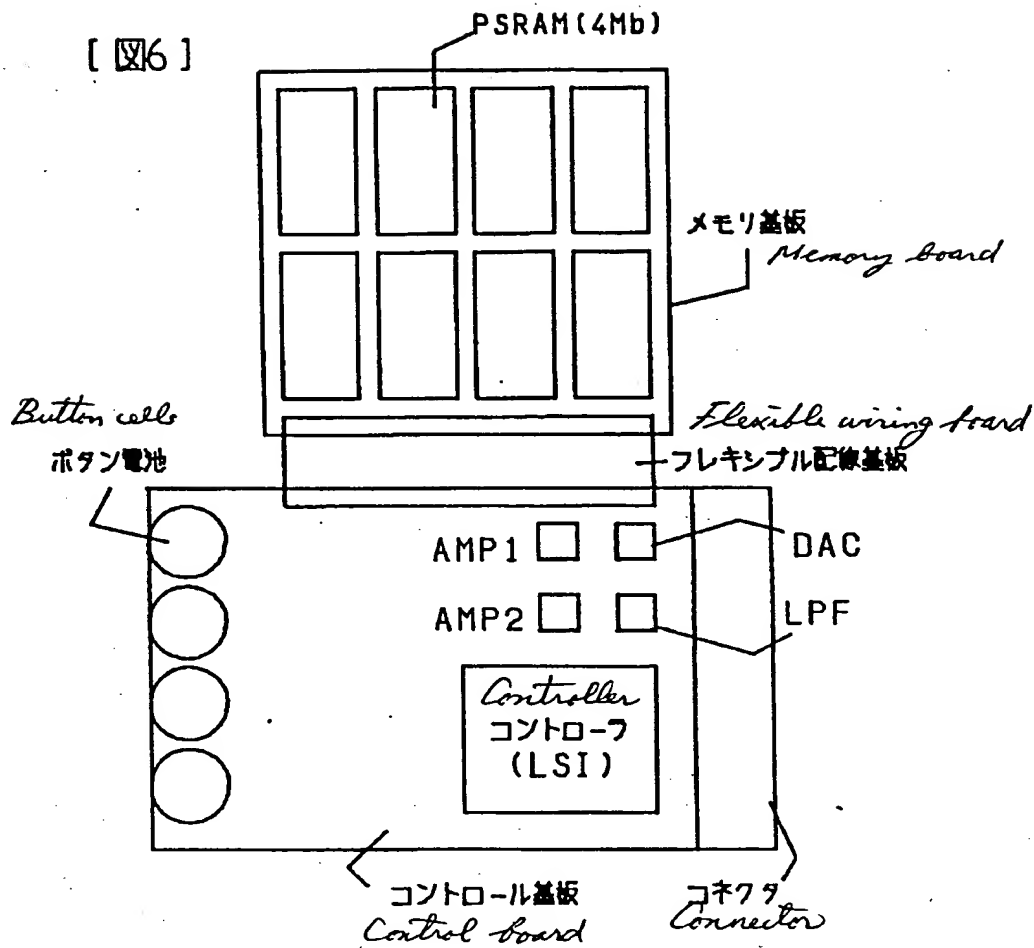
【図4】 [Fig. 4]

[ 図4 ]



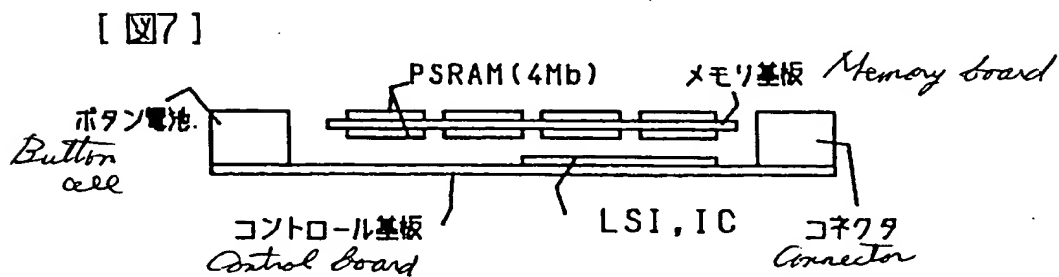
【図6】

[Fig. 6]



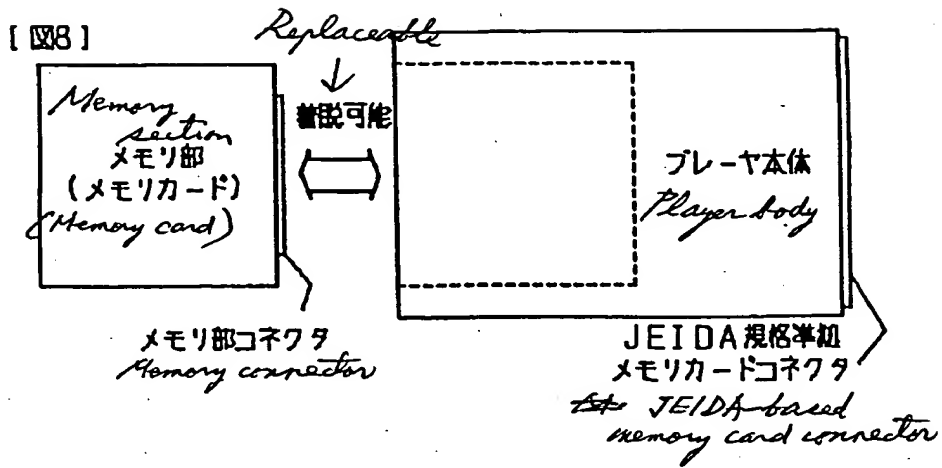
【図7】

[Fig. 7]

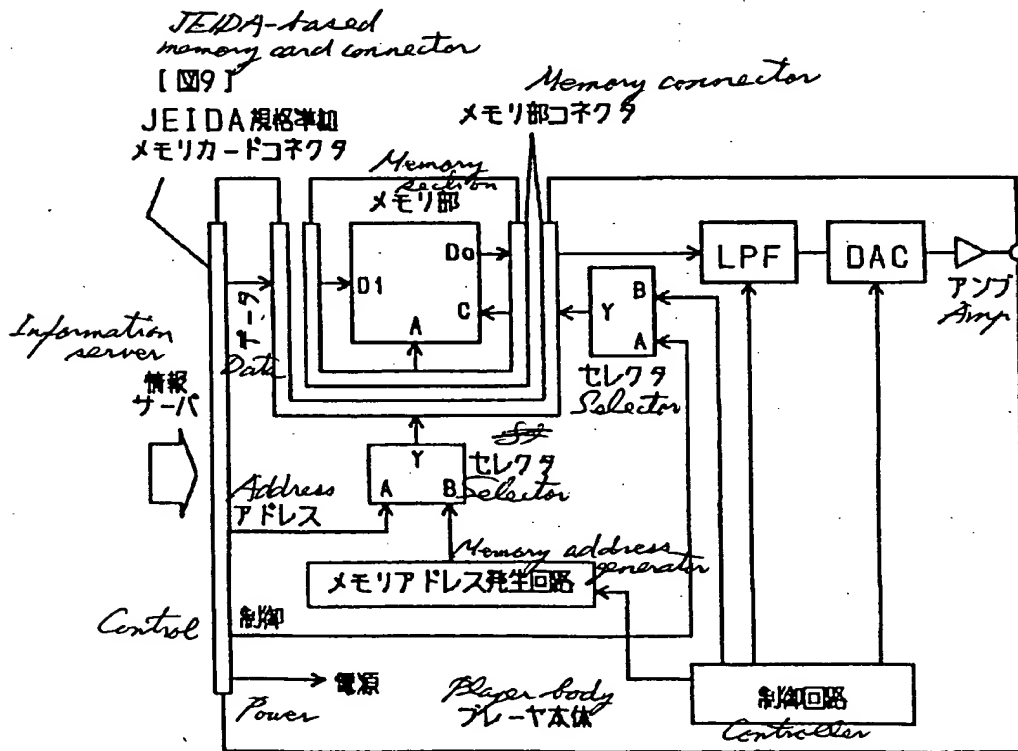


【図8】

[Fig. 8]

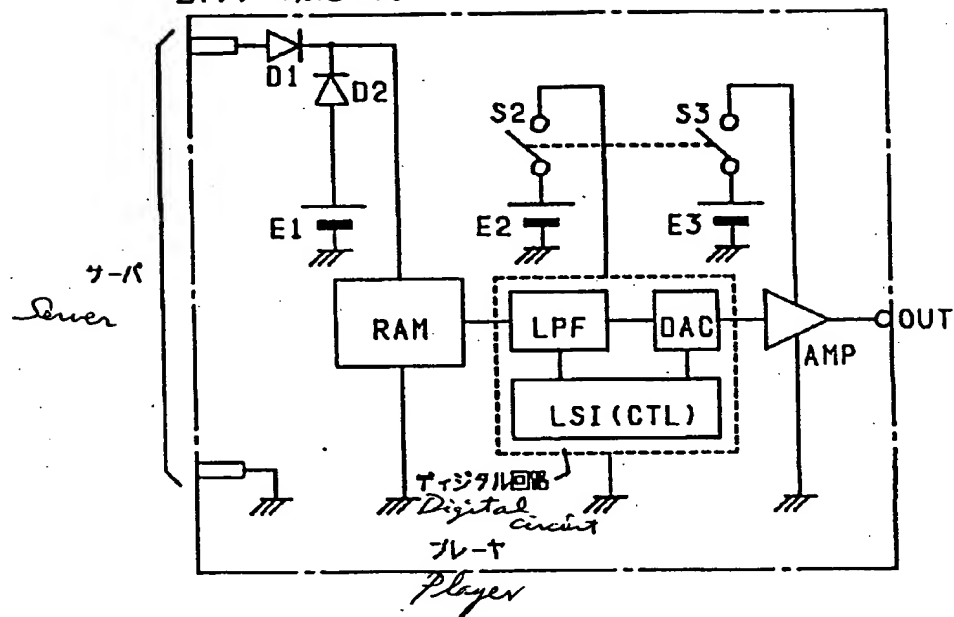


【図9】[Fig. 9]



[Fig. 10]

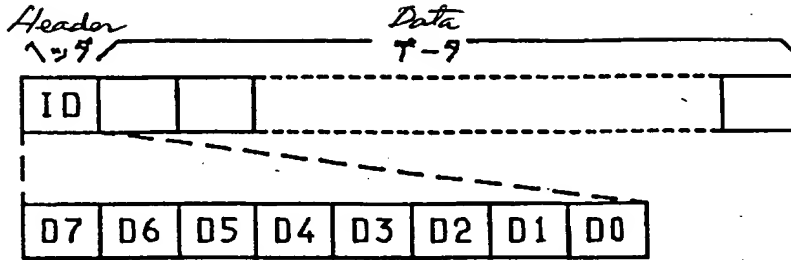
コネクター Connector



【図11】

[Fig.11]

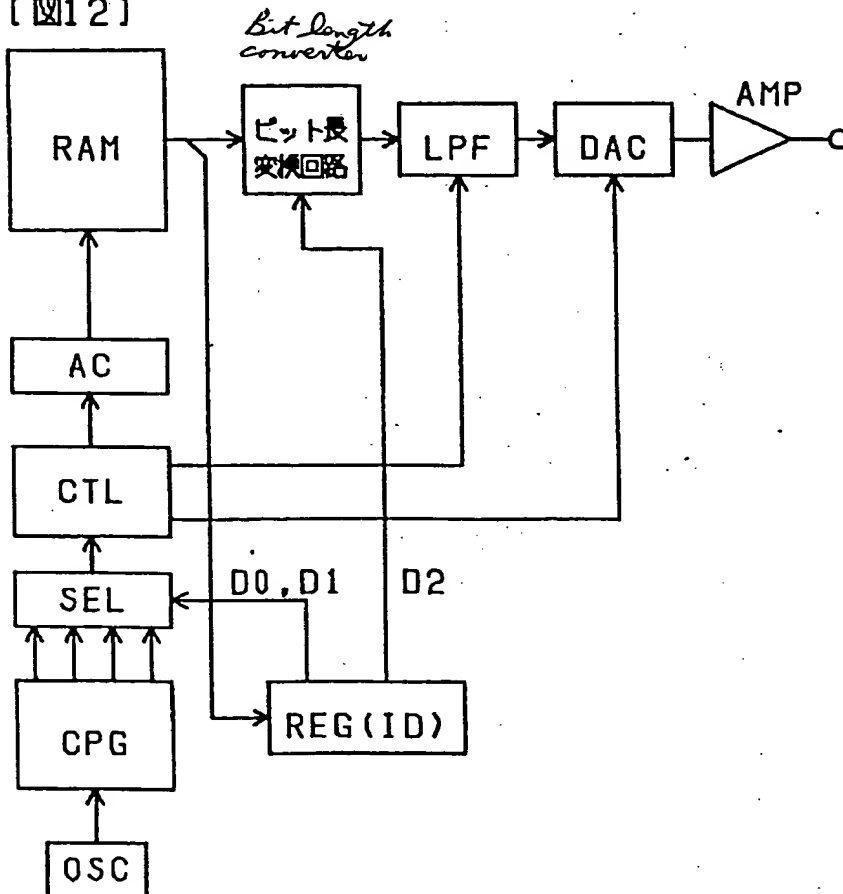
【図11】



【図12】

[Fig.12]

【図12】

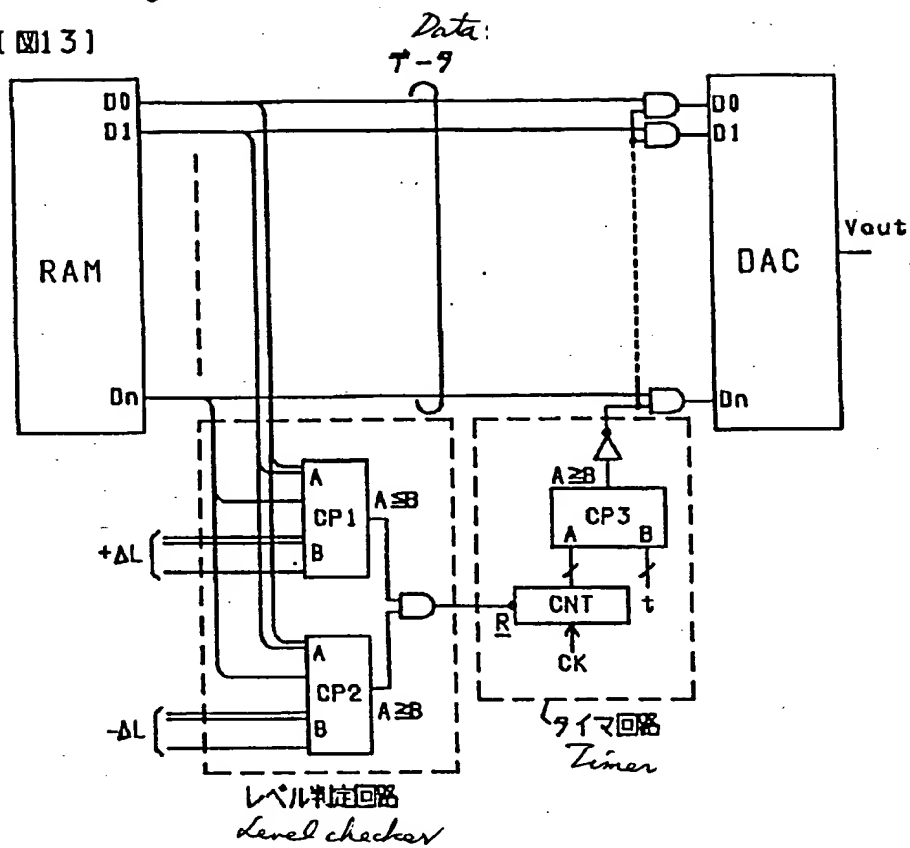




【図13】

[Fig. 13]

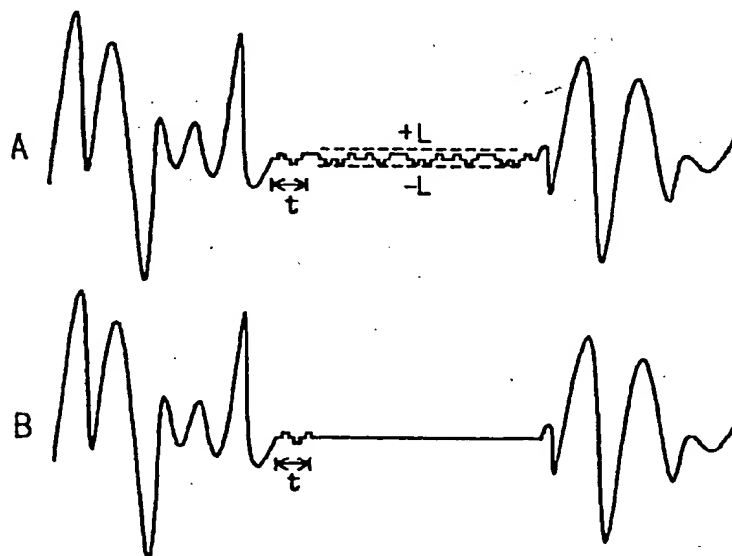
【図13】



【図14】

[Fig. 14]

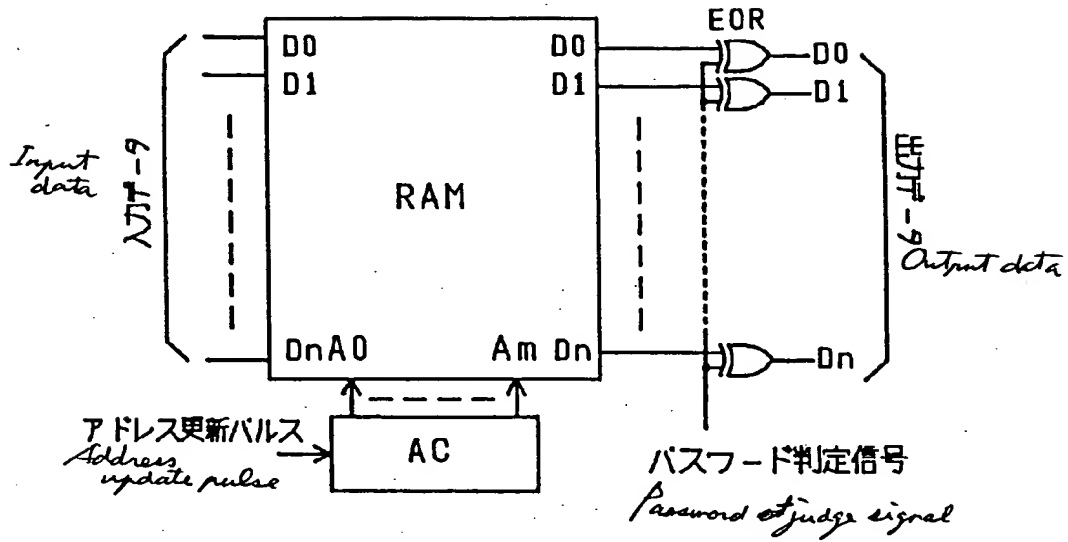
【図14】



【図15】

[Fig.15]

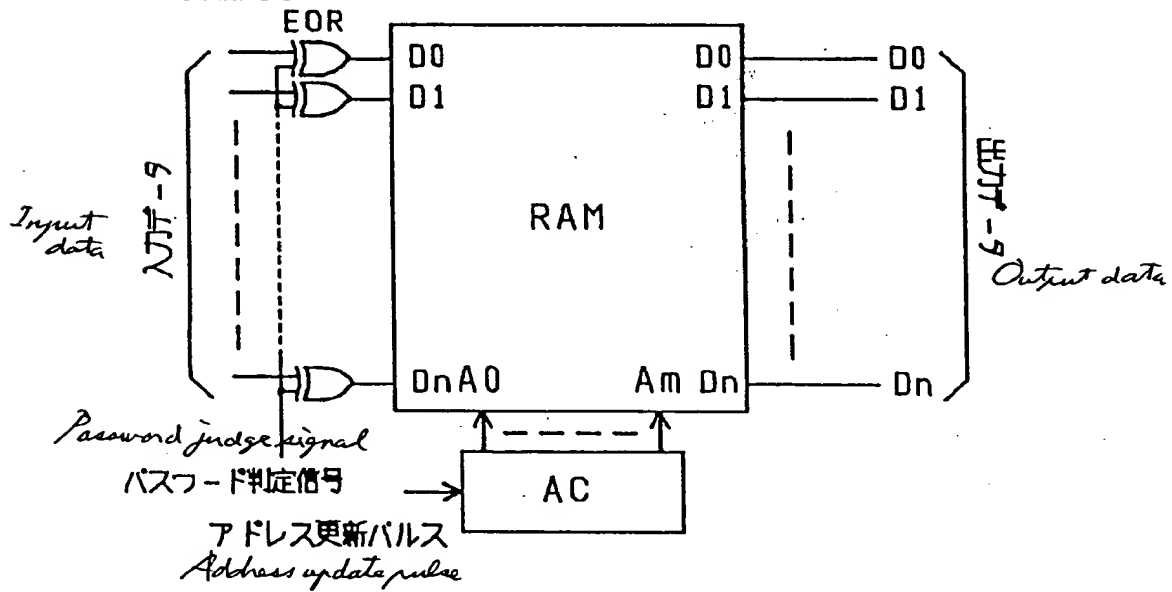
【図15】



【図16】

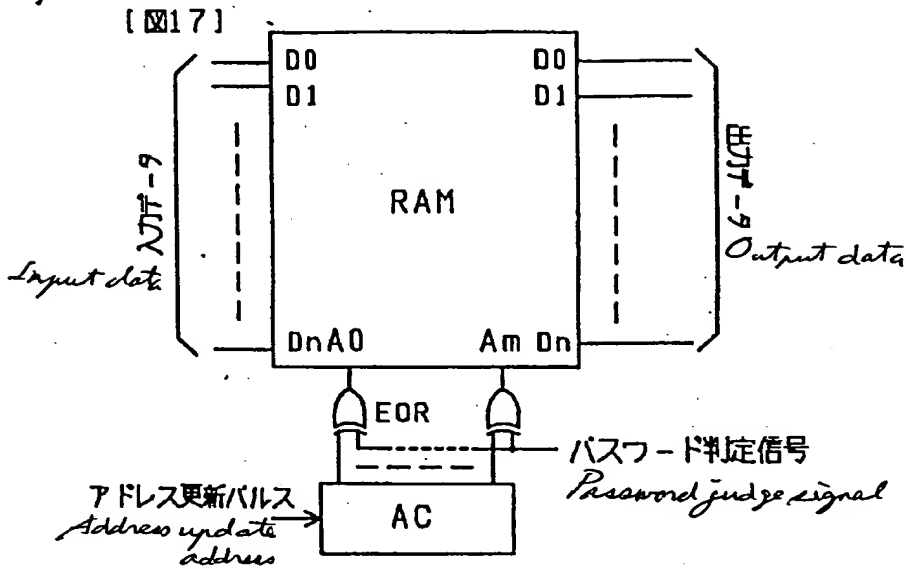
[Fig.16]

【図16】

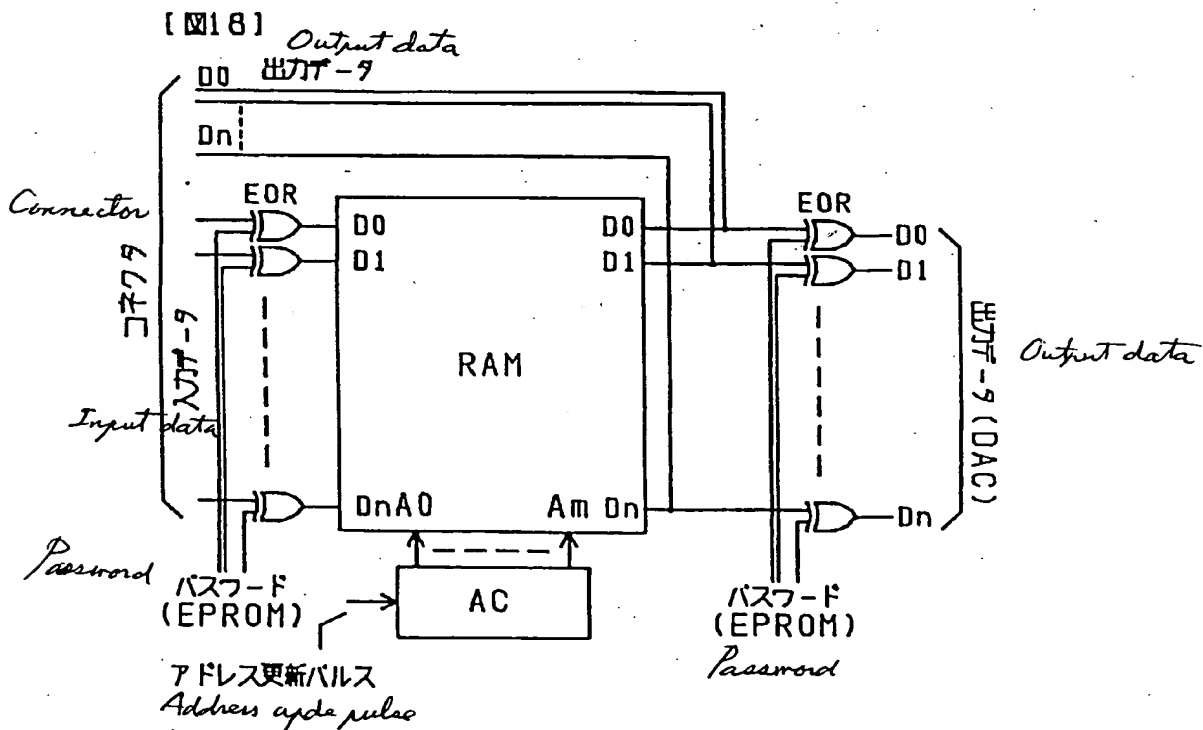




(Fig. 17) ~~Fig. 18~~ ~~Fig. 15~~



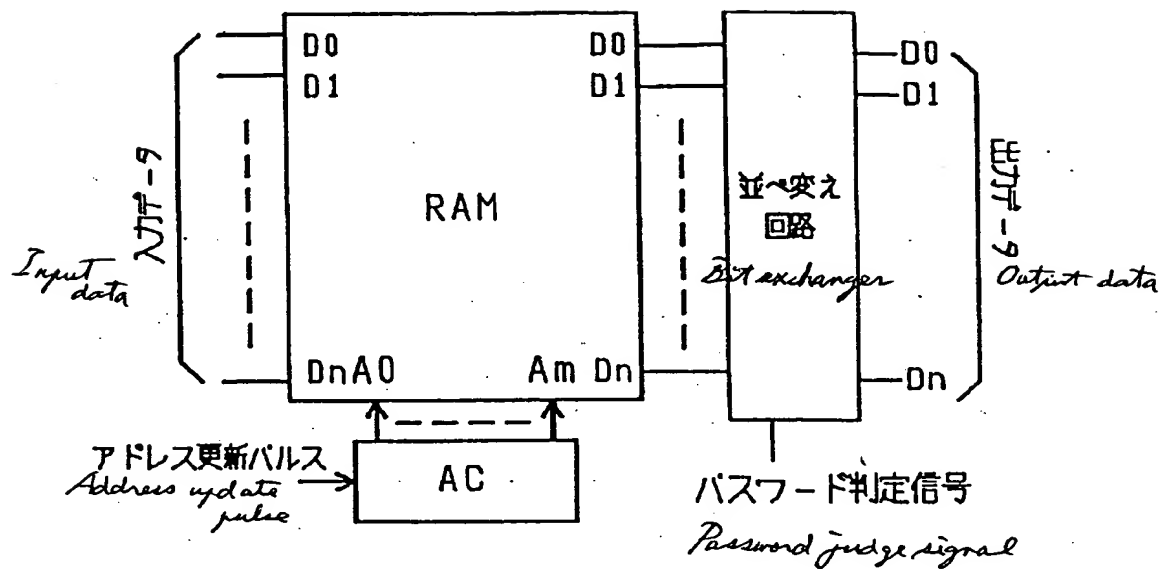
【図18】  
 [Fig. 18]



【図19】

[Fig. 19]

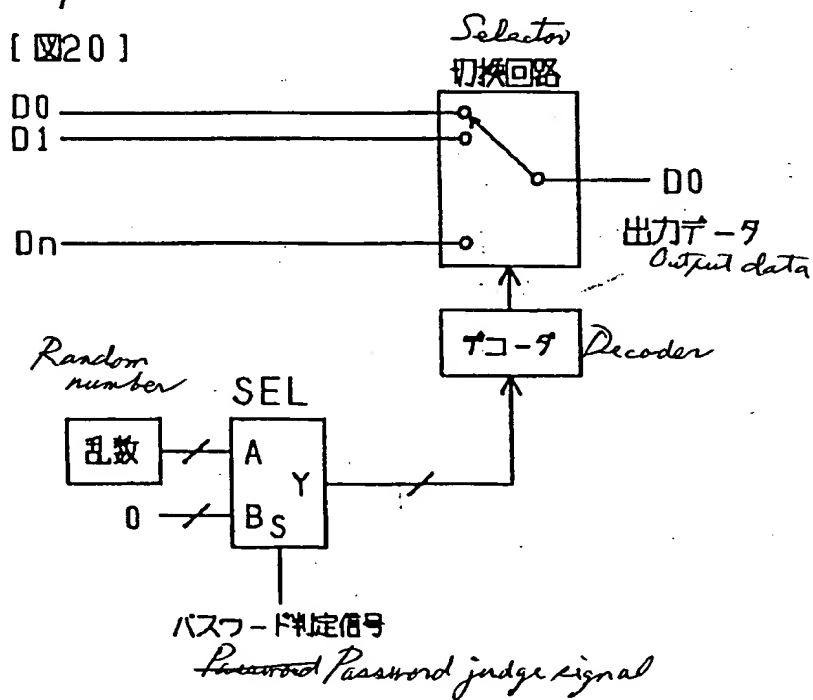
【図19】



【図20】

[Fig. 20]

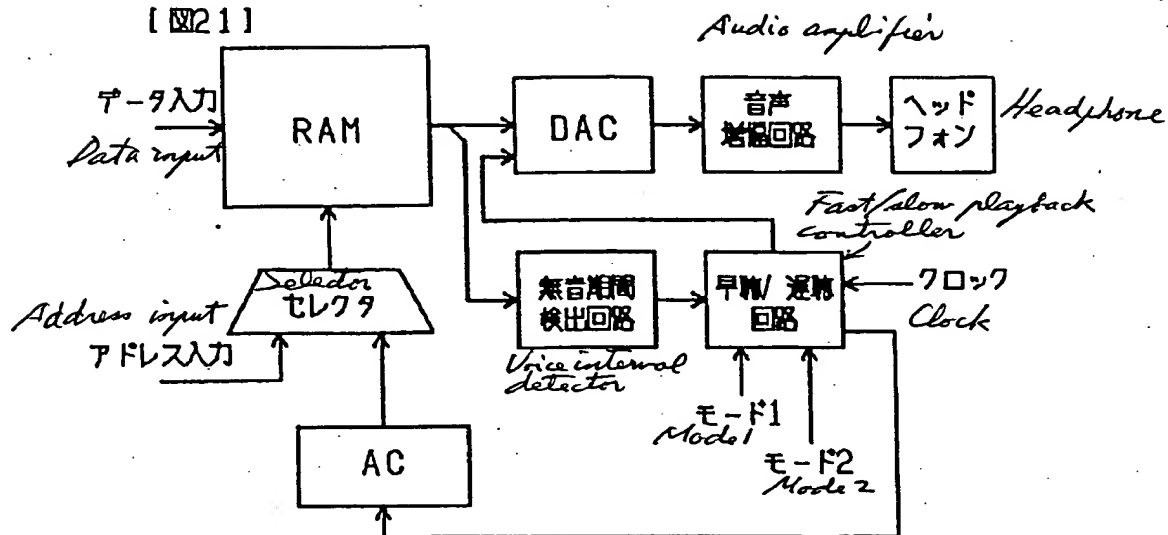
【図20】



【図21】

[Fig. 21]

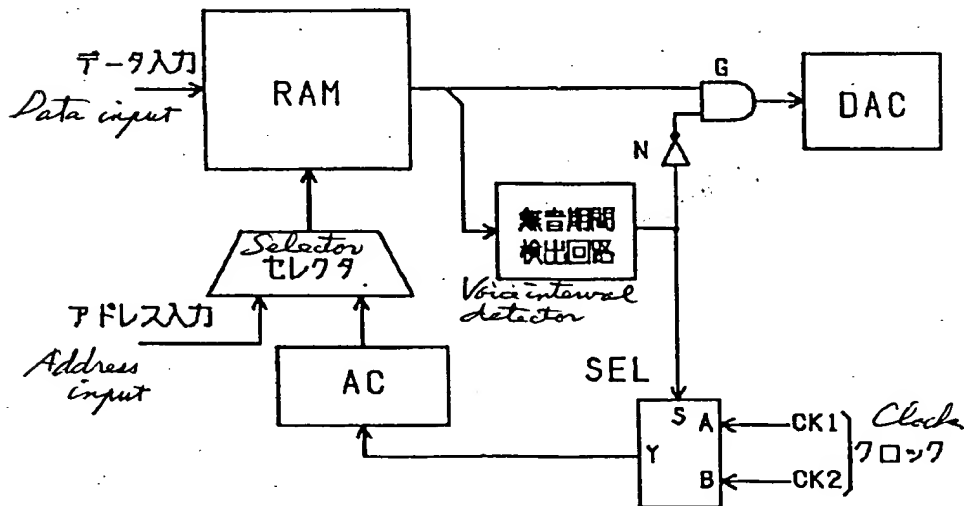
【図21】



【図22】

[Fig. 22]

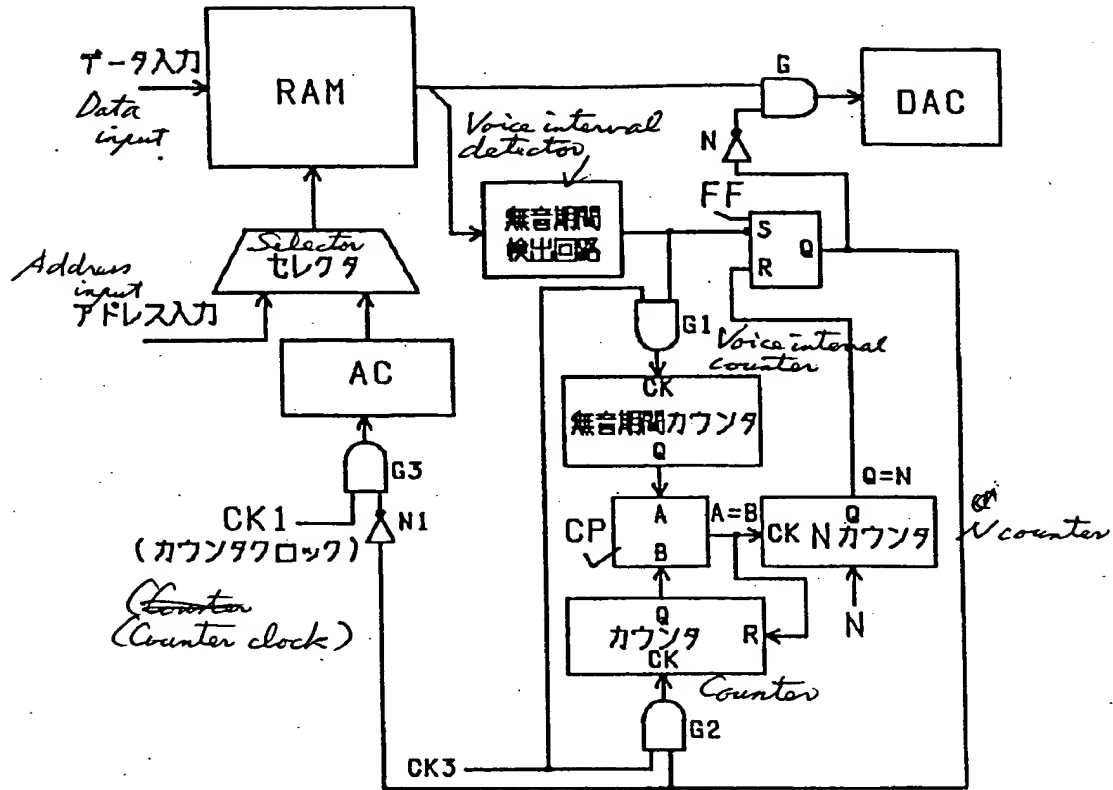
【図22】



【図 23】

[Fig. 23]

【図23】

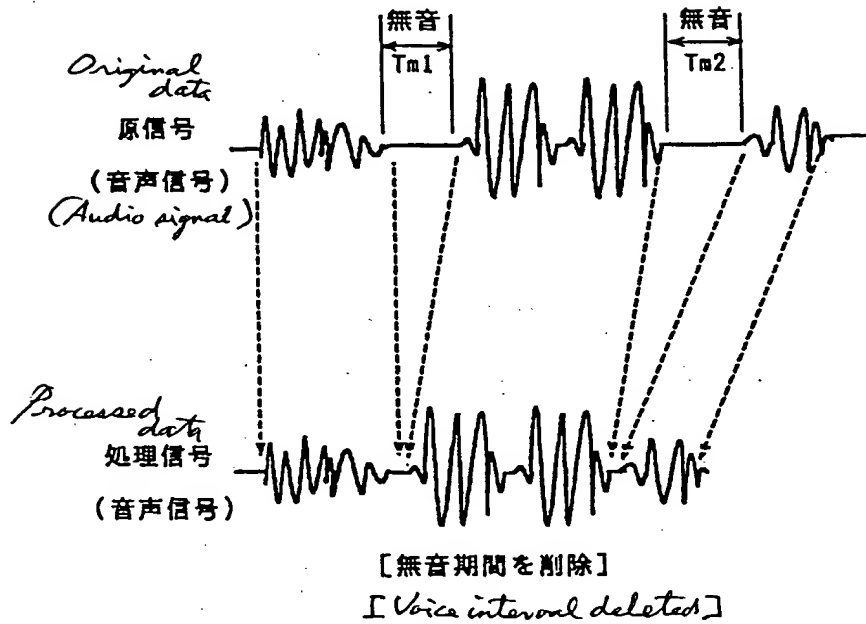


【図 2 4】

[Fig. 24]

【図 2 4】

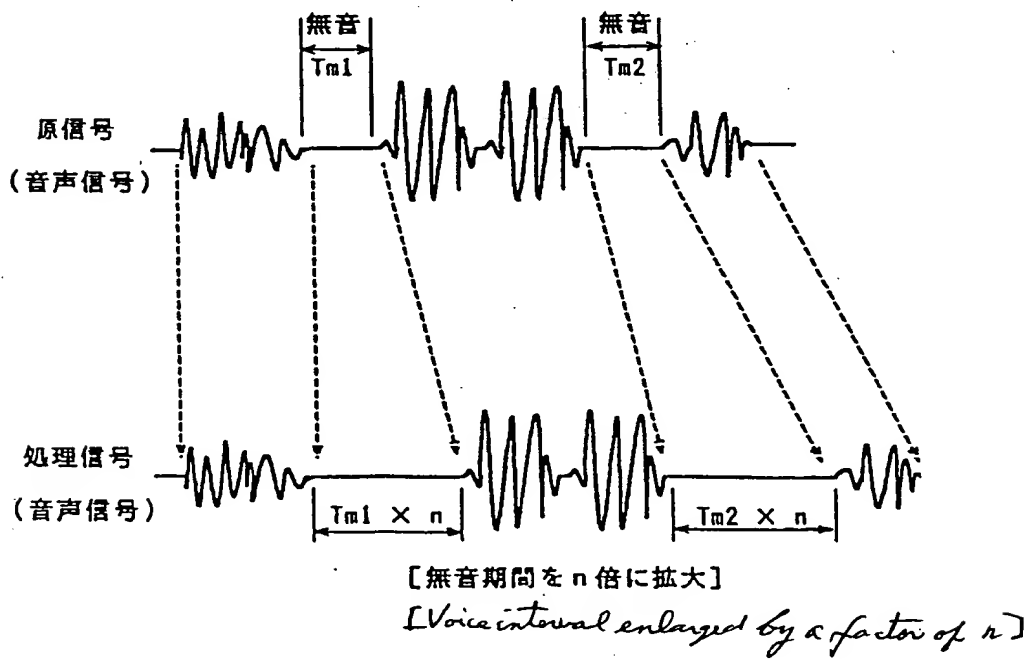
Voice interval



【図 2 5】

[Fig. 25]

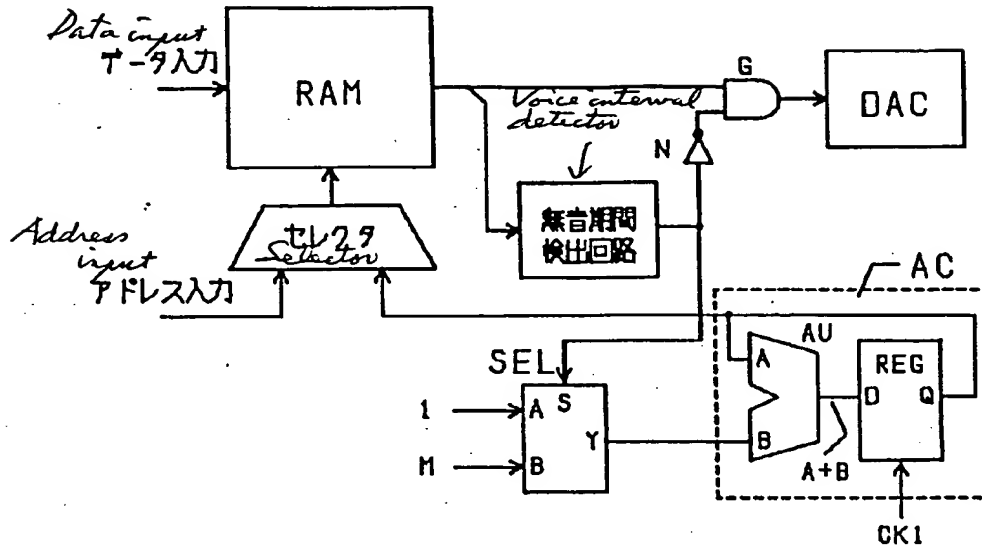
【図 2 5】



【図26】

[Fig. 26]

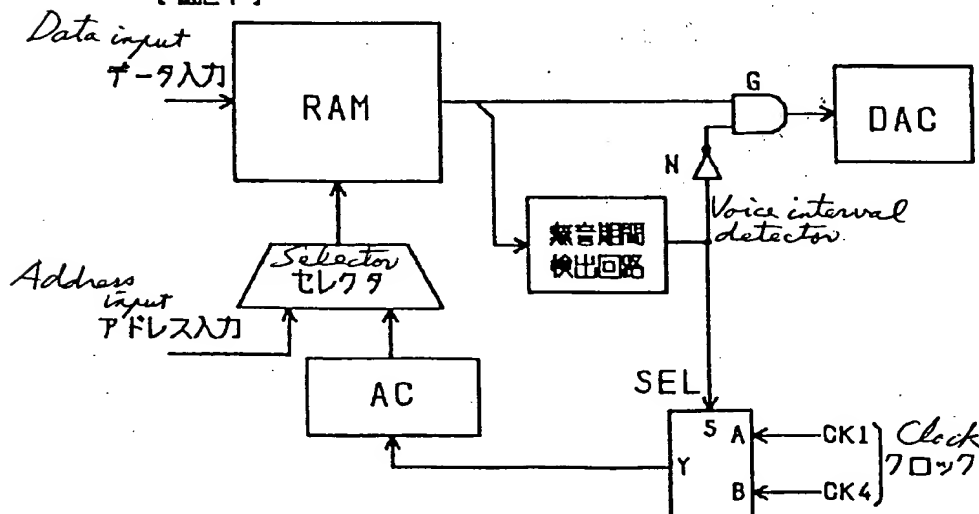
【図26】



【図27】

[Fig. 27]

【図27】





[Fig. 28]

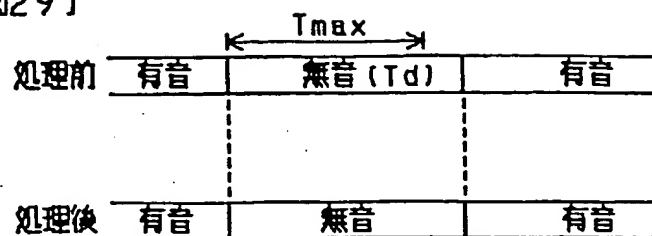
The diagram illustrates a digital circuit for voice interval detection and extension. The components and their interconnections are as follows:

- Data input** and **Address input** (アドレス入力) are inputs to the **RAM**.
- The **RAM** is connected to the **Voice interval detector** and the **無音期間検出回路** (Silence period detection circuit).
- The **Voice interval detector** is connected to the **DAC** via a gate **G** and a flip-flop **FF**.
- The **無音期間検出回路** is connected to the **無音期間カウンタ** (Silence period counter) and the **延長用カウンタ** (Extension counter).
- The **無音期間カウンタ** is connected to the **延長用カウンタ** via a gate **G1**.
- The **延長用カウンタ** is connected to the **MU** (Multiplexer) via a gate **G2**.
- The **MU** is connected to the **SEL** (Selector) via a gate **G3**.
- The **SEL** is connected to the **CP1**, **CP2**, and **CP3** (Counters) via a gate **G4**.
- The **CP1**, **CP2**, and **CP3** are connected to the **最大延長時間K** (Max extension time K).
- The **最大延長時間K** is connected to the **延長用カウンタ** via a gate **G2**.
- The **延長用カウンタ** is connected to the **無音期間カウンタ** via a gate **G1**.
- The **無音期間カウンタ** is connected to the **延長用カウンタ** via a gate **G1**.
- The **延長用カウンタ** is connected to the **MU** via a gate **G2**.
- The **MU** is connected to the **SEL** via a gate **G3**.
- The **SEL** is connected to the **CP1**, **CP2**, and **CP3** via a gate **G4**.
- The **CP1**, **CP2**, and **CP3** are connected to the **最大延長時間K**.
- The **最大延長時間K** is connected to the **延長用カウンタ** via a gate **G2**.
- The **延長用カウンタ** is connected to the **無音期間カウンタ** via a gate **G1**.
- The **無音期間カウンタ** is connected to the **延長用カウンタ** via a gate **G1**.
- The **延長用カウンタ** is connected to the **MU** via a gate **G2**.
- The **MU** is connected to the **SEL** via a gate **G3**.
- The **SEL** is connected to the **CP1**, **CP2**, and **CP3** via a gate **G4**.
- The **CP1**, **CP2**, and **CP3** are connected to the **最大延長時間K**.
- The **最大延長時間K** is connected to the **延長用カウンタ** via a gate **G2**.

【図 29】

[ Fig. 29 ]

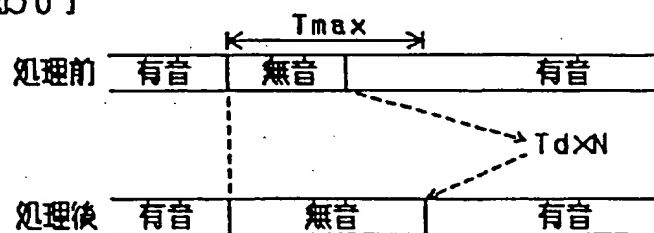
【図29】



【図 30】

[ Fig. 30 ]

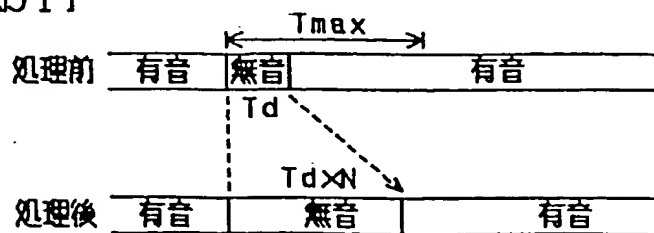
【図30】



【図 31】

[ Fig. 31 ]

【図31】

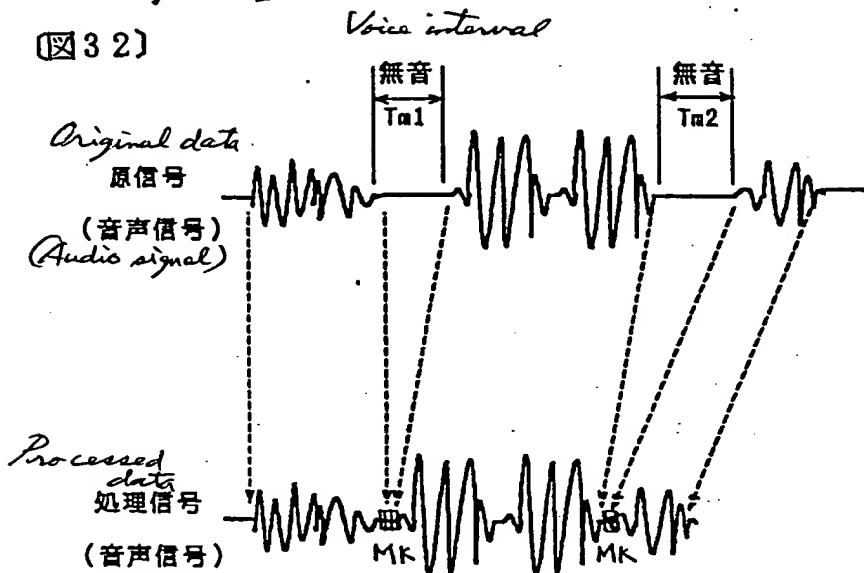


【書類名】 図面その3 [Title of Document]  
Drawing No. 3

【図 3 2】

[Fig. 32]

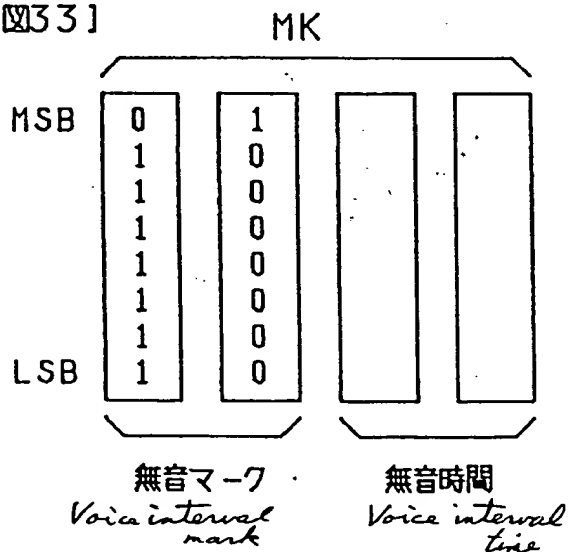
【図 3 2】



【図 3 3】

[Fig. 33]

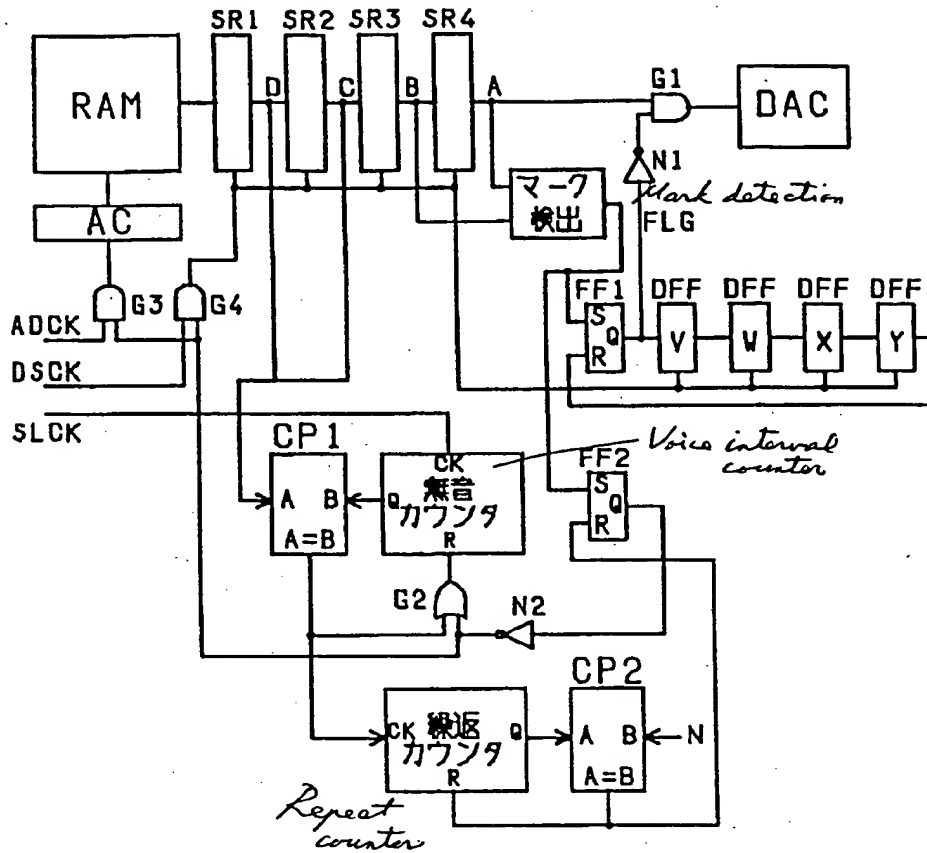
【図 3 3】



【図 34】

[Fig. 34]

【図 34】



[fig. 35]

The block diagram illustrates a digital control system for a motor driver. It consists of several interconnected components:

- Register (レジスタ)**: Receives a **Din** input and outputs a signal **Q** to the **Comparator**. It also has a set/reset input **S**.
- Comparator (コンパレータ)**: Compares inputs **A** and **B**. The output **A > B** is connected to the **CTL** block.
- Counter (カウンタ)**: Labeled **CAR**, it receives a clock signal **CK** and outputs a signal **Q** to the **Comparator**.
- Repeat Counter (リピートカウンタ)**: Also labeled **CAR**, it receives a clock signal **CK** and outputs a signal **DS** to the **CTL** block.
- CTL (Control Logic)**: A central logic block that receives inputs from the **Stroke** signal, **Strobe**, **EOC**, and the **Comparator**. It outputs signals to the **Register** (**S**) and the **Counter** (**CK**).
- LPF (Low Pass Filter)**: A dashed box containing a resistor **R** and a capacitor **C** to ground. It receives an input from the **CTL** block and produces the final output **Vout**.

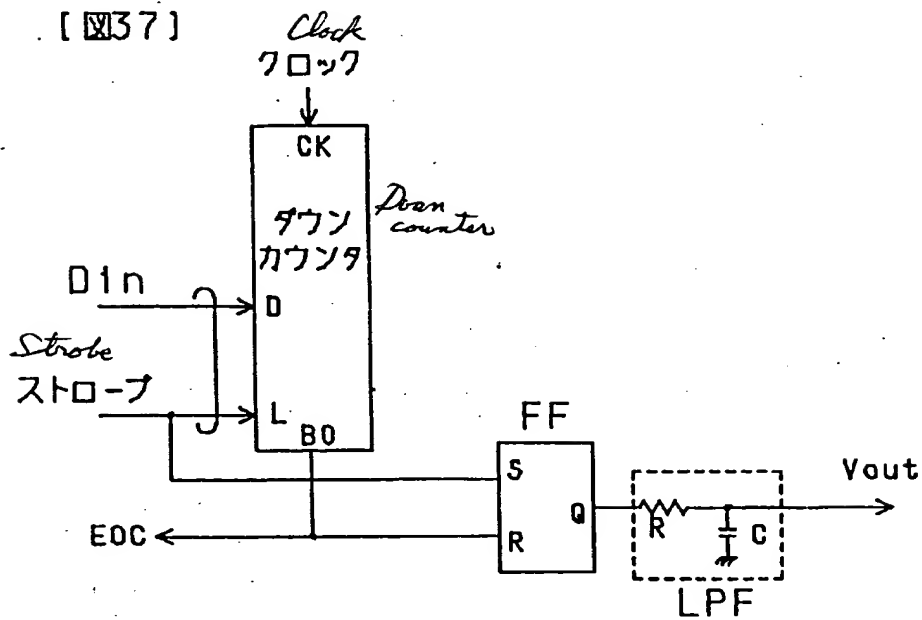
The system is clocked by a **CK (10MHz)** signal.

LF 19.36]

【図37】

[Fig. 37]

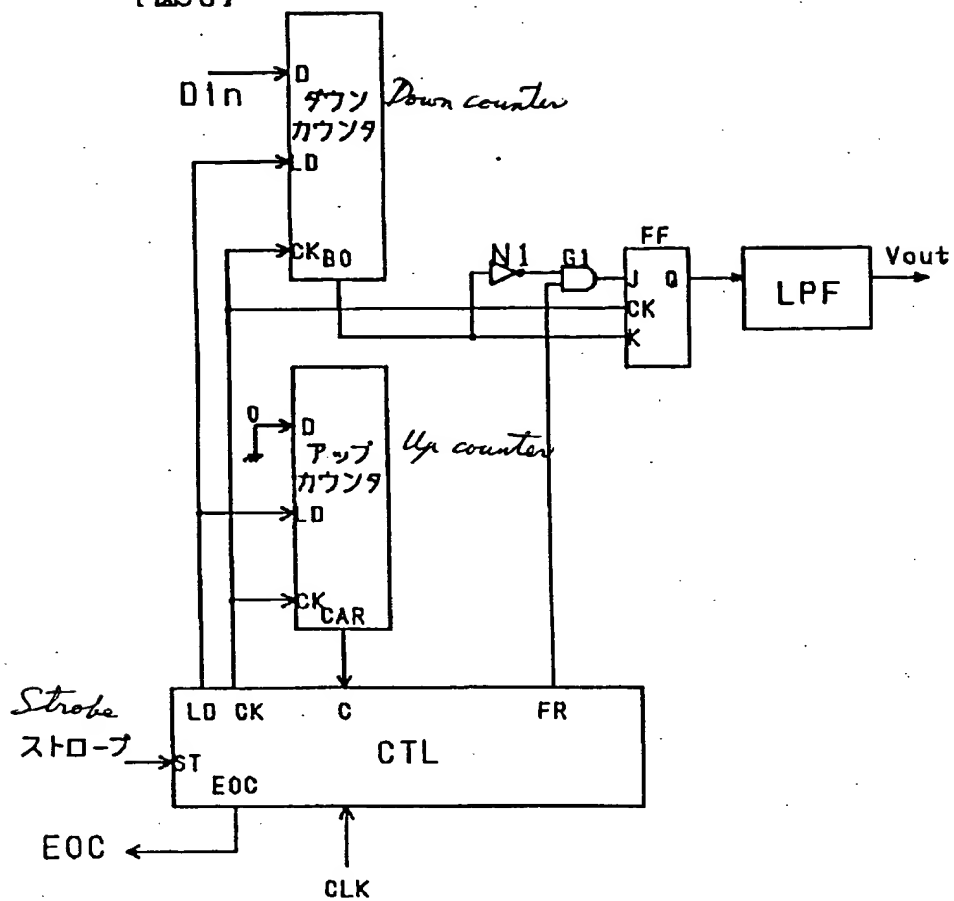
【図37】



【図38】

[Fig. 38]

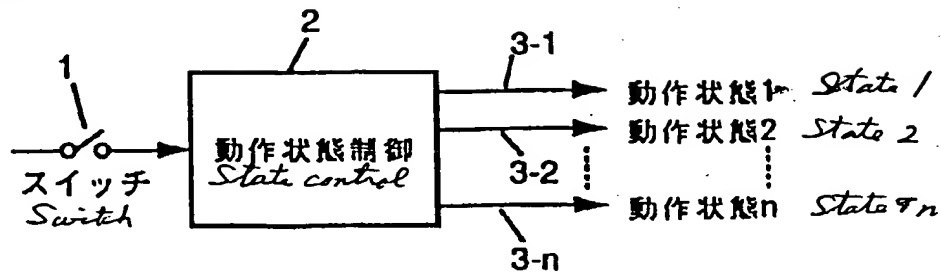
【図38】



【図39】

[Fig. 39]

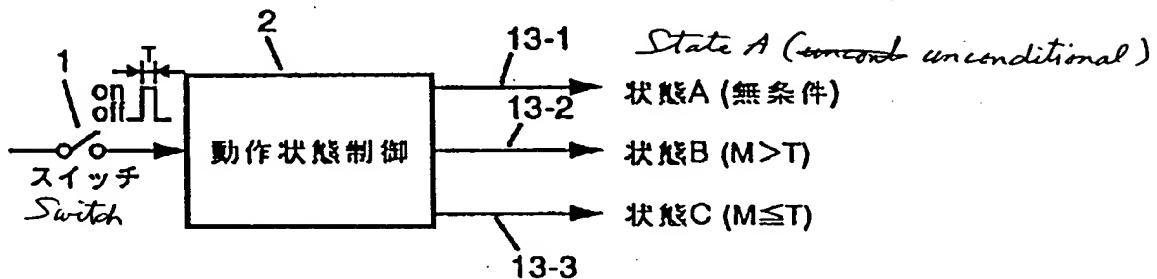
【図39】



【図40】

[Fig. 40]

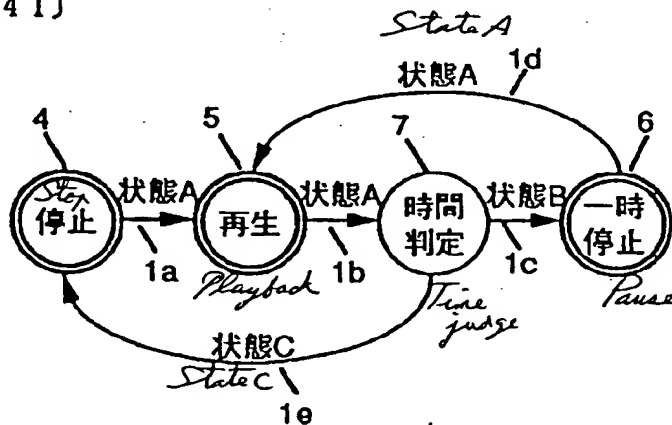
【図40】



【図41】

[Fig. 41]

【図41】

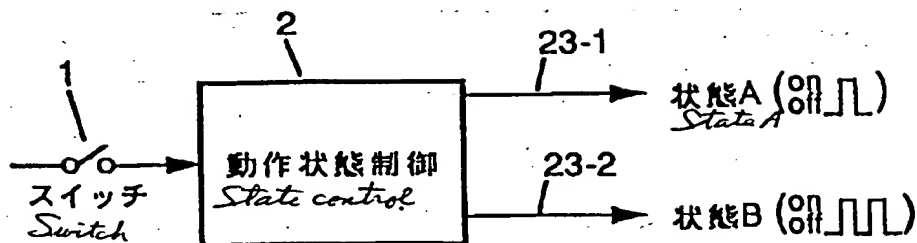




【図42】

[Fig. 42]

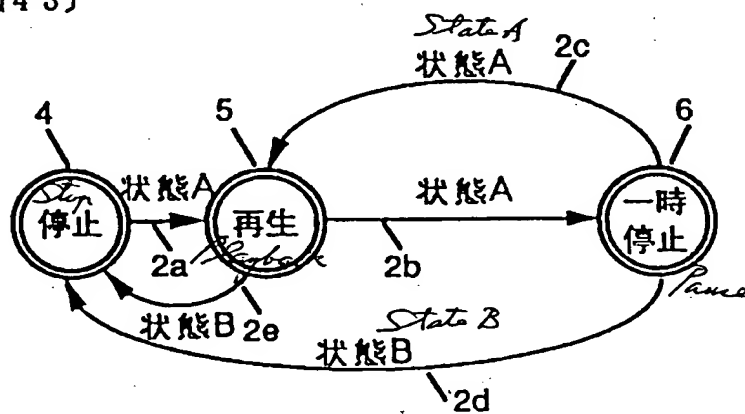
図42)



【図43】

[Fig. 43]

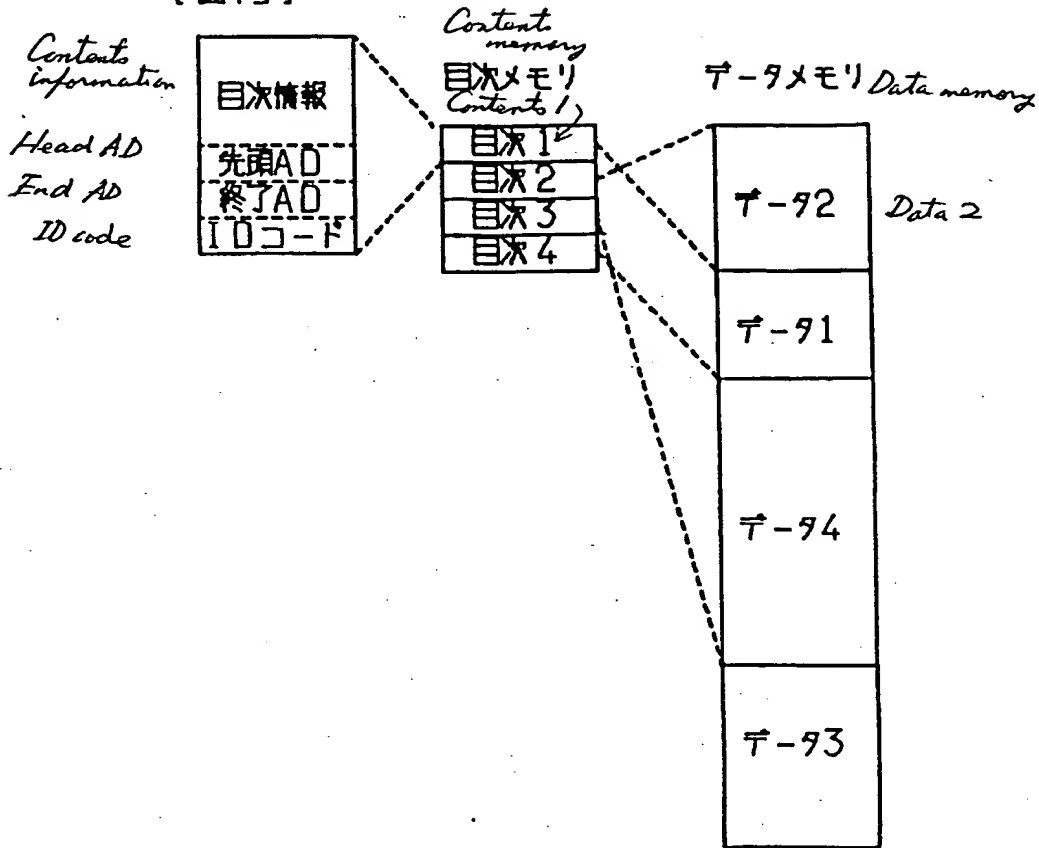
図43)



【図45】

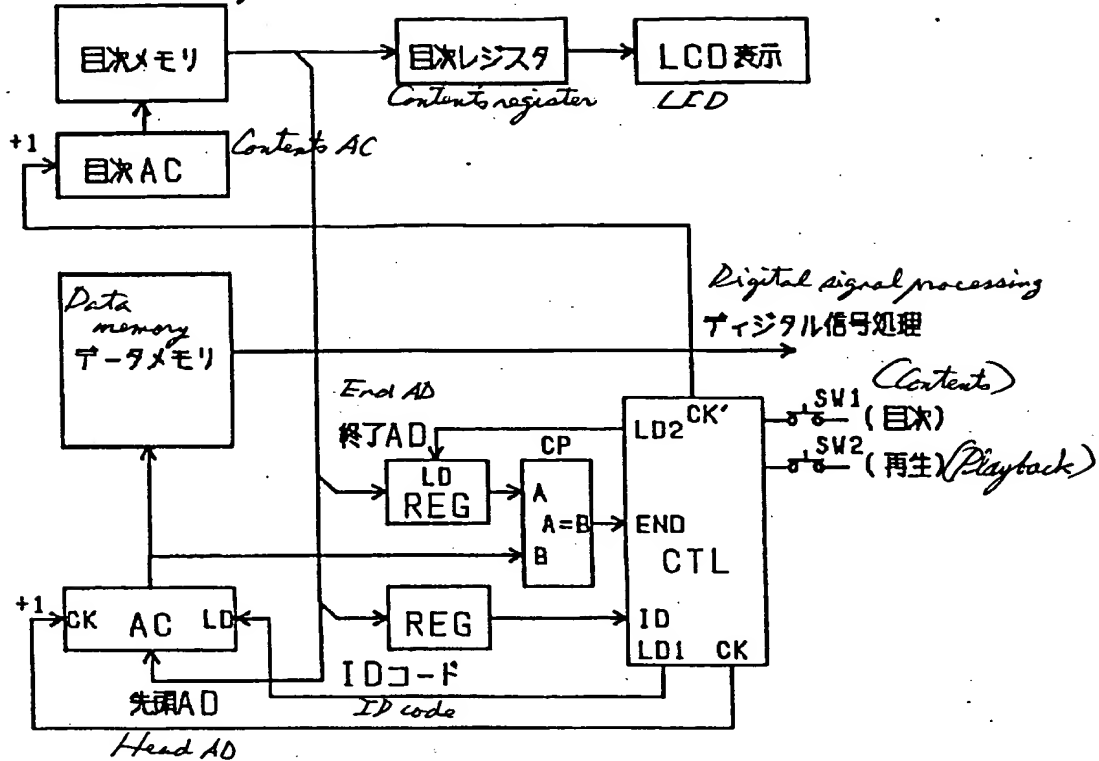
[Fig. 45]

【図45】



[Fig. 46] -

## Content memory





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DECLARATION

I, Michiyuki MORITA , a national of Japan, c/o Asamura Patent Office of 331-340, New Ohtemachi Building, 2-1, Ohtemachi-2-chome, Chiyoda-ku, Tokyo, Japan do hereby solemnly and sincerely declare:-

- 1) THAT I am well acquainted with the Japanese language and English language, and
- 2) THAT the attached is a full, true and faithful translation into the English language made by me of Japanese Patent Application No. 2-181402

The undersigned declares further that all statements made herein of his own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001, of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Signed this 31st day of January , 1994.

Michiyuki Morita

Michiyuki MORITA

2-181402

APPLICATION FOR PATENT

July 11, 1990

The Director-General  
The Patent Office

Title of the Invention: INFORMATION STORAGE AND  
REPRODUCTION SYSTEM AND METHOD  
OF STORAGE AND REPRODUCTION

Number of Claim(s) for a Patent: 11

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List of the annexed documents:

- (1) Specification ----- 1 copy
- (2) Drawings ----- 1 copy
- (3) Power of Attorney ----- 1 copy
- (4) Duplicate of Application Form ----- 1 copy

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                                  Tokyo, Japan.

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                  Address:    - do. -

                 Name:      Katsutaka KIMURA  
                  Address:    - do. -

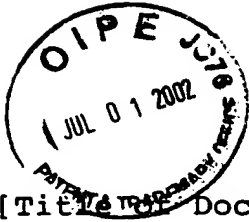
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3-57930

1 [Title of the Document] Specification

[Title of the Invention] DATA CONVERSION SYSTEM AND  
DATA CONVERTER

[Scope of Claim for a Patent]

5 [Claim 1] A data conversion system characterized  
in that the difference between an immediately preceding  
sampling data and an input data is determined, and when  
the result thereof is larger than the maximum value of a  
compressed code, the maximum value of the compressed  
10 data is outputted, while when the result is smaller than  
the maximum value of the compressed data, the result of  
subtraction is outputted by the compressed data.

[Claim 2] A data conversion system according to  
Claim 1, characterized in that the compressed data is  
15 extended to the original data by being added to the  
immediately preceding sampling data.

[Claim 3] A data converter characterized by  
including a subtractor for determining the difference  
between an input data and an immediately preceding  
20 sampling data stored in a register, a comparator for  
comparing the subtraction output with the maximum value  
of the compressed data, and a selector for outputting the  
above-mentioned maximum value when the subtraction  
output is larger than the maximum value by the output of  
25 the comparator, and outputting the subtraction output by

1 the compressed data when the subtraction output is  
smaller than the maximum value.

[Claim 4] A data converter according to Claim 3,  
characterized in that the register is such that the  
5 output signal of an adder for adding the compressed data  
outputted from the selector to the immediately preceding  
stored data is retrieved as an immediately preceding  
sampling data.

[Claim 5] A data converter characterized by  
10 including a register having a bit length corresponding  
to the original data as an extender of a compressed data  
for determining the difference between an immediately  
preceding sampling value and an input sapling data,  
assuming the maximum value of the compressed data when  
15 the result of subtraction is larger than the maximum  
value, and assuming the result of subtraction by the  
compressed data when the result of subtraction is  
smaller than the maximum value, and an adder for adding  
the output signal of the register to the compressed data  
20 to form a new data of the register, wherein an extended  
data is obtained from the output of the adder or the  
register.

[Detailed Description of the Invention]

[0001]

25 [Industrial Field of Utilization]

The present invention relates to a data  
conversion system and a data converter, or in particular



1 to an effective technique used for a digital audio  
circuit.

[0002]

[Prior Art]

5 In digital audio technique, a code is compressed in order to lengthen the sound recording time or for a similar purpose. The amplitude and frequency distribution of an acoustic signal changes greatly, though comparatively gently, with time. In this connection, a method of coding for changing the quantization  
10 step width in accordance with the characteristics of neighbouring signals is an adaptive PCM (APCM). In this adaptive PCM, the quantization step width is changed in accordance with the amplitude of the quantization value  
15 of an immediately preceding sample. The adaptive difference PCM, on the other hand, is the result of introduction of the adaptive step width into the difference PCM, wherein a signal is not directly quantized but the difference with a predicted value is quantized as  
20 an application. And,  $\Delta M$  is a method of coding for quantizing a signal with one bit. According to this method, the strain increases with a sharp signal change. The adaptive  $\Delta M$ , by contrast, is such that the quantization step width is increased when the same code is  
25 sustained, while it is decreased if the code is inverted.

In relation to this code conversion technique, there is available "Digital Audio Dictionary", pp. 26 to

1 28, compiled by Japan Audio Association, and published  
by Ohm, July 25, 1987.

[0003]

[Problem that the Invention is to Solve]

5 In the adaptive PCM, the adaptive difference  
PCM and the adaptive  $\Delta M$ , a multiplier is required for  
changing the step width. Also, a complicated circuit  
such as a microcomputer or a digital signal processor is  
required, thereby leading to the disadvantage of an  
10 increased circuit scale. Another shortcoming of  $\Delta M$  is a  
large quantization strain resulting in an insufficient  
fidelity.

The object of the present invention is to  
provide a data conversion system and a data converter  
15 capable of achieving a high fidelity with a simple  
configuration.

The above-mentioned and other objects and  
novel features of the present invention will become  
apparent from the description in the present specifica-  
20 tion and the accompanying drawings.

[0004]

[Means for Solving the Problem]

A representative example of the invention  
disclosed in the present application will be briefly  
25 explained. Specifically, the difference between an  
immediately preceding sampling data and an input data is  
determined, and when the difference is larger than the  
maximum value of a compressed code, the maximum value is

1    outputted, while when the difference is smaller than the  
     maximum value, the result of subtraction is outputted to  
     produce a compressed data. Also, the difference between  
     an input data and an immediately preceding sampling data  
5    stored in a register is determined by a subtractor, and  
     the output of subtraction is compared with the maximum  
     value of a compressed code by a comparator. A selector  
     is controlled by the comparison output. A circuit is  
     used in which when the subtraction output is larger than  
10   the maximum value, the particular maximum value is  
     outputted, while when the subtraction output is smaller  
     than the maximum value, the subtraction output is  
     outputted.

     [0005]

15        [Operation]

     According to the means described above, the  
     amplitude and the frequency distribution of an acoustic  
     signal changes comparatively gently with time. By using  
     a data conversion system as described above, therefore,  
20   data compression and extension high in fidelity is made  
     possible. Also, this data compression and extension can  
     be realized by a simple combination of logic circuits  
     including a subtractor, an adder, a comparator and a  
     register.

25        [0006]

     [Embodiments]

     Fig. 1 is a block diagram showing an  
     embodiment of a data converter configured of a data

1 conversion system according to the present invention.

The data converter according to this embodiment, though not specifically limited, is for converting an analog signal into a 16-bit digital signal and is  
5 intended for a circuit for compressing and outputting the digital data as an 8-bit digital data.

The analog signal  $V_{in}$  is inputted to the analog-to-digital converter ADC and is converted into a digital data of  $n$  bits (16 bits, for example, as  
10 mentioned above). This embodiment uses a circuit described below for compressing the digitally-converted 16-bit data into a data of  $m$  bits (8 bits, for example).

[0007]

One of the inputs of the subtractor is  
15 supplied with the 16-bit data  $D_1$  digitally converted as above. The other input of the subtractor is supplied with a 16-bit data  $D_2$  stored in the register. The 16-bit data  $D_2$  stored in the register is assumed to be an immediately preceding sampling data as described later.  
20 The subtractor subtracts the immediately preceding sampling data  $D_2$  stored in the register from the input data  $D_1$  digitally converted, and outputs the difference ( $D_1 - D_2$ ) therebetween as a data  $D_3$ . The difference data  $C$  is supplied to an input  $B$  of the comparator. The  
25 other input  $A$  of the comparator is supplied with a data  $D_4$  corresponding to the maximum value of an 8-bit data to be compressed. This data  $D_4$  is comprised of 16 bits of 0000000011111111 (255 in decimal notation) as shown

1 with all the least significant eight bits (m) as 1.

[0008]

The comparator compares the data D3 and D4 supplied to the input terminals A and B, and when B is larger than A ( $D3 > D4$ ), forms a high-level output signal, while when A is larger than B, generates a low-level output signal. The output signal of the comparator is used as a selection signal.

An input A of the selector is supplied with an 8-bit maximum value data d4 to be compressed (11111111), and the input B with a data d3 representing the least significant eight bits of the difference data D3. The selector selects and outputs the maximum value data d4 of the input A when the output signal of the comparator is at high level, i.e., when the subtraction data D3 is larger than D4, and the data d3 of the least significant eight bits of the subtraction output supplied to the input B when the output signal of the comparator is at low level, i.e, when the subtraction data D3 is smaller than D4.

[0009]

The output signal d5 of the selector, though not specifically limited, is stored in the memory, and read and outputted as a compressed 8-bit digital data Dout. The output signal d5 of the selector is supplied to one of the inputs of the adder. The other input of the adder is supplied with the output data D2 of the register. As a result, the adder adds the compressed

1 data d5 outputted from the selector to the immediately  
preceding sampling data D2 stored in the register, so  
that the sampling data D2' updated and assumed to be  
immediately preceding to the next input data D1 is  
5 formed and stored in the register. In this way, the  
accumulation error is prevented by generating the next  
sampling data by the register and the adder.

Subsequently, the 16-bit (n-bit) input data D1  
is converted into an 8-bit (m-bit) compressed data d5 by  
10 repeating similar processes.

[0010]

Fig. 2 shows waveforms for explaining the  
operation of analog-to-digital conversion accompanied by  
the data compression described above.

15 At the time of data compression, the register  
is cleared of data (0000000000000000). As a result,  
when an analog signal rises sharply as shown, the  
progressive adding operation of the least significant 8-  
bit maximum value would fail to follow an input digital  
20 signal. Once the difference between the input digital  
signal and the immediately preceding sampling data is  
reduced below the maximum value of the compressed data,  
however, it is possible to obtain a compressed data  
faithfully corresponding to the input signal change. As  
25 for an acoustic signal which has an amplitude and a  
frequency distribution changing comparatively gently  
with time, data compression is possible with a fidelity  
posing no practical problem.

1 [0011]

Fig. 3 is a block diagram showing another embodiment of a data converter in a data conversion system according to the present invention. This

5 embodiment is intended for a circuit in which a data compressed into m bits (eight bits, for example) as in the aforementioned embodiment is extended into an n-bit (16-bit) data and at the same time is outputted by being converted into an analog signal.

10 The data Din compressed by a data compressor as shown in Fig. 1, though not specifically limited, is transferred and stored in a memory. The memory the data d5 read out of the memory is supplied to an input of the adder. The other input of the adder is supplied with an  
15 n-bit data D6 stored in the register. The adder forms a data D7 by adding the data d5 to D6. This data D7, though not specifically limited, is inputted to the register. The data D6 outputted from the register and extended is inputted to the digital-to-analog converter  
20 DAC to form a demodulated analog signal Vout.

[0012]

The operation of the data extender will be explained. At the time of starting the data extending operation, the register is cleared as in the afore-  
25 mentioned case. The compressed data d5 read out of the memory is added to an immediately preceding n-bit data D6 of the register each time of reading, and is stored in the register as expanded data. As a result, the

1 expanded data is restored which changes in steps in  
accordance with the change components due to the  
compressed data d5 as shown in Fig. 2.

[0013]

5 A block diagram of the essential parts of a  
digital signal receiving/delivery system according to an  
embodiment of the present invention is shown in Fig. 4.  
The digital signal receiving/delivery system, though not  
specifically limited, is intended for a system to  
10 commercialize and sell information of a digital signal.  
In other words, the sale of the information is made  
available as one of forms of receiving/delivery of a  
digital signal.

In Fig. 4 is shown a block diagram of a  
15 terminal device of a digital signal selling system.  
This terminal device is equivalent to a vending machine  
for cigarettes or soft drinks such as juice and  
functions as an information server. The terminal device  
is connected to an original supplier of a digital signal  
20 through a broad band integrated services digital network  
(B-ISDN) to receive the digital signal as a commodity  
without specific limitation. As a result of employment  
of this system, the digital signal is transferred only  
to a specified terminal device through a communication  
25 network in a manner similar to such commodities as  
cigarettes and juice. In this case, the digital signal  
as a commodity can be transferred at high speed and in a  
great amount, free of any traffic jam or air pollution



1 unlike in the case of general commodities. The terminal  
device is installed in front of a store like a station  
booth, a cigar stand or a book shop.

The terminal device is roughly comprised of an  
5 input section, a memory section and an output section.  
Each circuit block, which is connected to a VME bus, is  
adapted to receive digital and various control signals.  
This terminal device, which is connected to a player  
shown by dotted line in Fig. 4, is used to directly  
10 receive a specific digital signal as a commodity in the  
form of electrical signal.

[0014]

Fig. 5 is a block diagram showing an input  
section of the terminal device. The input section of  
15 the terminal device has a digital input interface INF  
for the broad band integrated services digital network  
(B-ISDN) and an analog input interface (right and left  
analog inputs) for receiving an input signal in an  
analog form. The analog input interfaces are provided  
20 with low-pass filters LPF, associated with the right  
input Rin and the left input Lin, for eliminating  
extraneous frequency band components contained in the  
analog input signals Rin and Lin in advance, respec-  
tively. These input signals Rin and Lin are alternately  
25 selected through a multiplexer MPX with respect to time,  
introduced to a sample-and-hold circuit S/H and  
converted into a digital signal by an analog-to-digital  
converter ADC. At this time, the analog-to-digital

1 converter ADC outputs two-channel (stereo) time-shared  
digital signals of right and left channels in time  
series, which signals are introduced to the digital  
input interface. This input interface INF has a data  
5 converter built therein for data compression. Such  
analog input interfaces are used for digitalizing and  
storing music programs, regular news, stock market  
information, various commodity market situations or the  
like sent by broadcasting in a memory.

10 A monaural signal is inputted as the above-  
mentioned right or left input signal. The function may  
be added to broaden band widths of the low-pass filters  
LPF for input signals having a broad band widths such as  
music, and to narrow the band widths of the low-pass  
15 filters LPF for input signals having narrow band widths  
such as news. INCT designates an input section  
controller, and NIF indicated by dotted line a network  
interface corresponding to the B-ISDN.

[0015]

20 Each analog input interface may be adapted to  
receive a message from an automatic answering telephone  
set by being connected to a telephone line. In such a  
case, the function of a telephone set may be added to  
the terminal device connected with the automatic  
25 answering telephone set to receive a recorded message  
therefrom. When the analog input interface is used in  
this way, the message transfer time is undesirably  
lengthened. If a subscriber to a digital line system

1 uses a digital automatic answering telephone set to  
store messages in a digital form and compresses a data  
by a data converter as mentioned above, the messages  
recorded can be received in a very short time, and by  
5 doing so, the user can confirm the messages, at the  
desired time while being in transportation means or  
under the like situation.

[0016]

Fig. 6 is a block diagram showing an  
10 embodiment of the memory section in the terminal device.  
This memory section includes an external memory like a  
hard disk memory HDD, a RAM (random access memory) as a  
buffer memory, a ROM (read only memory) for storing  
various programs, and a microprocessor CPU for  
15 processing information or performing control operations  
in accordance with these programs. The programs include  
the information-processing program for a digital or  
analog input operation, a data exchange operation with  
the hard disk memory HDD, a display operation of a  
20 liquid crystal display LCD or a data transfer operation  
with a player connected to the output section. The RAM,  
though not specifically limited, has a storage capacity  
of approximately 1 MB (megabyte as referred to in the  
same way hereinafter), and the ROM a storage capacity of  
25 approximately 512 KB (kilobyte as referred to in the  
same way hereinafter). The hard disk memory HDD, though  
not specifically limited, has a storage capacity of  
approximately 250 MB, and has a function as a backup

1 memory in case of power failure or interception. In  
addition, it functions like a warehouse for storing a  
great variety of digital signals. This hard disk memory  
HDD, which is connected to an internal bus through a  
5 hard disk controller HDDC, is adapted to write and read  
data in response to an instruction from the micro-  
processor CPU. In this case, if a data compressed by a  
data-conversion system is stored as mentioned above, a  
high-quality acoustic data of 16 bits may be stored as a  
10 8-bit data, for example, and therefore the storage  
capacity is doubled.

[0017]

The LCD is a liquid crystal display and is  
used for displaying information menu, operating  
15 instructions, etc. The surface of the LCD with a touch-  
key function is used for selecting one of the displayed  
menu, display switching, etc. When the player is  
connected, for example, (1) Music, (2) news, (3) Weather  
forecasting, (4) Stock market situation, (5) Reading,  
20 etc. are displayed as the first information menu on the  
display screen. If one of them, say, (2) News is  
selected, the screen is shifted to display (1) NHK, (2)  
FEN, (3) Traffic information, (4) Sports news, etc. By  
designating a desired one of these news programs, a  
25 digital signal corresponding to the selected program is  
received by the player.

1           In a case of (1) Music, for instance, such  
music categories as classic, popular and jazz are  
displayed, so that if a specific music category is  
selected, a name of a marketable music is displayed.  
5   Such music information, though not specifically limited,  
is assumed to be stored in a specific area of the hard  
disk memory or the ROM. When the desired music is not  
available in the hard disk memory HDD, the device is  
connected to an original supplier of digital signals  
10 through the communication channel B-ISDN to transmit an  
intended music program to the player. The LCD, which is  
connected to the internal bus through an LCD controller  
LCDC, is used for the above-mentioned display and  
corresponding input operations through the touch keys.  
15           A bus interface VMEINF is a VME bus interface  
for connecting the internal bus and the VME bus to each  
other.

[0018]

          The news, the stock market situation and the  
20 like, which are required to be replaced by the latest  
information with the lapse of time, are stored in a  
buffer memory BM included in the output section as  
described later. As a result, the information can be  
directly transferred to the player without accessing the  
25 hard disk memory HDD on each occasion. Also, the music  
program, if large in sales amount, may be stored in the  
buffer memory BM. In this case, the top ten items in

1 sales volume of each music category may be displayed as  
a display menu to facilitate selection by the user.

[0019]

The output section of the terminal device  
5 includes an output interface OUTINF connected to the VME  
bus, a player controller ACTL, a buffer memory BM, a  
monitor controller MOCTL, a monitor MONT, etc, as shown  
in Fig. 7. The output section has a connector for  
connection with the player and is connected to the  
10 player through the connector for receiving a digital  
signal as a commodity. The buffer memory BM has a  
comparatively large storage capacity of approximately 96  
MB, which is equivalent to about ten times as large as  
the maximum storage capacity 8 MB of the player 101 as  
15 described later.

The monitor MONT, though not specifically  
limited, has a speaker and a headphone output and is  
used for reproducing a starting part of a given music  
selected from the music program. The monitor MONT and  
20 the monitor controller MOCTL used in this configuration  
are equivalent to those used in the playback circuit of  
the player described later.

[0020]

As explained above, cigarettes and juice sold  
25 by the vending machine are encased in a package or a  
container and sold integrally therewith. Commercialized  
information or the like, on the other hand, are sold by  
use of, with paper or a floppy disk or an IC memory as a

1 medium functioning as a package or a container. A music  
program is also offered for sale in a form integrated  
together with a storage medium such as magnetic tape or  
compact disk. These media have no commercial value of  
5 their own. Only in combination with an "electronic  
notebook", a personal computer or the like terminal  
device, information is retrievable and processed as a  
commodity. Also, the value of a music program as a  
commodity is exhibited only in combination with a  
10 cassette tape recorder or other reproducing device.

In contrast, a digital signal receiving/  
delivery system according to the present invention is  
such that a digital signal as a commodity/is received in  
the form of electrical signal without any intermediary  
15 of a storage medium functioning as the container  
mentioned above. For the purpose of receiving of the  
digital signal in the form of electrical signal in this  
way, a memory circuit RAM is mounted on the player as  
described later. A digital signal introduced to this  
20 memory circuit RAM can be reproduced through a playback  
circuit of the player as a unit. Specifically, the  
received commodity directly exhibits the value thereof  
as a commodity. These two features make the present  
invention conspicuously different from the conventional  
25 commodity transactions. Further, according to a system  
in which the player is connected to the terminal device  
and in which a digital signal is transmitted and  
received as a commodity as described above, only the

1 required information can be specified and sold when  
required.

In the case of using a data conversion system  
according to the present invention, a long-time storage  
5 or a storage of a plurality of types of program is made  
possible by a RAM comparatively small in storage capacity  
without deteriorating the fidelity of the audio signal  
reproduced.

[0021]

10 In Fig. 7, POW designates a power supply,  
which, though not specifically limited, supplies power  
from the terminal device to the player for the purpose  
of transmitting a high-speed digital signal. Also, in  
the case where a rechargeable secondary battery is used  
15 as a power supply of the player in place of the primary  
battery, the circuit is used also for changing the  
secondary battery rapidly by the power supply. Signals  
transferred between the output section and the player  
are an operating voltage V, a digital signal D, an  
20 address signal A, a control signal C or a status signal  
S, etc.

[0022]

A block diagram of an embodiment of the player  
is shown in Fig. 8.

25 The player is roughly comprised of a large-  
scale integrated circuit LSI constituted by a gate  
array, a memory circuit RAM for storing a digital  
signals, and a playback circuit. The memory circuit



1 RAM, though not specifically limited, includes a pseudo-  
static RAM (PSRAM) having a storage capacity of about 8  
MB. As described later, for example, sixteen pseudo-  
static RAMs of about 4 megabits are mounted to realize  
5 the storage capacity of about 8 MB described above. The  
large-scale integrated circuit LSI has mounted thereon a  
controller CTL, an address counter AC, a multiplexer MPX  
and a data converter DC. The controller forms various  
control signals for playback operations of the digital  
10 signal stored in the memory circuit RAM and a control  
signal used for data input to the memory circuit RAM.

The address counter AC generates an address  
signal for reading the digital signal stored in the  
memory circuit RAM. The multiplexer MPX switches  
15 between the address in accessing the memory circuit RAM  
from the server (terminal device) and the address in  
accessing the memory circuit RAM inside thereof. More  
specifically, a digital signal is written into the  
memory circuit RAM in accordance with the address from  
20 the server side, while information is read for playback  
operation of the particular digital signal in accordance  
with the address generated from the address counter AC.

[0023]

The data converter has dual function of  
25 extending to the original data and changing the bit  
length of the digital data stored in the memory RAM  
which is in compressed form. LPF designates a low-pass  
filter including a digital filter circuit for inputting

1 only the band component required for playback to the  
digital-to-analog converter. According to this  
embodiment, as described later, a digital signal of a  
plurality of sampling rates is handled in accordance  
5 with the information or program involved. The pass band  
of the digital filter is switched in accordance with  
these sampling rates. The digital-to-analog converter  
has the function of outputting analog signals for the  
right and left channels so separated in accordance with  
10 the stereo signals inputted in time division. In the  
case where the digital signal is monaural, the same  
analog signal is outputted from the two channels. The  
player is adapted to generate an audio output from the  
headphone in order to reduce the size and weight  
15 thereof. Outputs R and L represent a headphone  
terminal.

[0024]

A plan view of an embodiment of the packaging  
board configuring the player is shown in Fig. 9. The  
20 player includes a control board and a memory board. The  
control board has mounted along the longitudinal ends  
thereof power supply section with button cells inserted  
therein and a connector section. The board surface  
between the power supply section and the connector  
25 section has mounted thereon semiconductor integrated  
circuit devices or the like making up the large-scale  
integrated circuit LSI, amplifier devices AP1, AP2, a  
low-pass filter LPF and a digital-to-analog converter

1 DAC. The connector is conforming to the JEIDA standard  
(a standard for memory card and the like). The power  
supply section includes button cell holders and can be  
packaged with four alkali button cells (LR44). The size  
5 of this control board, though not specifically limited,  
is set to 52 mm by 82 mm so as to be accommodatable in  
the existing IC card case.

The memory board covers the area other than  
the comparatively thick parts of the connector section  
10 and the power supply section of the control board, and  
has mounted eight PSRAMs on each side thereof. The  
memory board and the control board are connected with  
each other by a flexible wiring board. In other words,  
the two boards are openable in two directions, right and  
15 left, to facilitate inspection and repair.

[0025]

Fig. 10 shows a side view of the package board  
as housed in a case. The memory board is folded over  
through the flexible wiring board on the surface area of  
20 the control board other than the power supply section  
and the connector section. As a result, the accommoda-  
tion in a case equivalent to the existing IC card (RAM  
card) is made possible, while at the same time realizing  
a small, thin player.

25 [0026]

A block diagram of an embodiment of the power  
supply system for the player is shown in Fig. 11. The  
player, as described above, is comprised of a memory

1 circuit RAM, a controller CTL made up of a digital  
circuit, a digital filter LPF, a digital-to-analog  
converter DAC and an amplifier AMP for outputting an  
analog signal. Each of these circuit blocks has a  
5 different operating voltage. The memory circuit RAM,  
for instance, requires a comparatively high operating  
voltage of about 4 V when a pseudo-static RAM is used as  
mentioned above. In contrast, the use of a CMOS circuit  
gate array or the like in a digital circuit makes  
10 possible an operation at a comparatively low voltage of  
about 3 V. The amplifier circuit AMP for driving the  
headphone is operable even at a lower operating voltage  
of about 1.5 V. As a result, except for the battery E1  
for supplying the memory RAM for holding information  
15 steadily, the voltages of the batteries E2 and E3 are  
supplied to each corresponding circuit through the power  
switches S2 and S3 by use of the batteries E1, E2  
adapted for the operating voltages of the respective  
circuits.

20 [0027]

In this way, the battery life is lengthened by  
supplying power to the directly associated circuits by  
use of a plurality of types of batteries having  
different voltage values. If the internal power supply  
25 is set to the highest voltage of 4 V, for instance, a  
wasteful current flows in the digital or analog circuit  
AMP, thereby to increase the current consumption. If  
the voltage of 4 V is supplied through an internal

1 voltage drop circuit, the current consumption in the  
voltage drop circuit would shorten the battery life.  
According to the present embodiment, in contrast, power  
is supplied through a selected battery having the  
5 required minimum capacity for each circuit, and  
therefore the wasteful current consumption is decreased,  
thereby substantially lengthening the battery life.

[0028]

If the writing of a digital signal into the  
10 memory circuit RAM or the reading of a digital signal  
therefrom is to be speeded up, the operating current of  
the memory circuit RAM must be increased. For this  
purpose, the server (terminal device) is provided with  
power supplying connectors for supplying an operating  
15 voltage of about 5 V higher than the internal voltage.  
In this case, in order to automatically switch the power  
between the battery and the server sides, the connector  
and the battery E1 are used to supply a voltage to the  
power terminal of the memory circuit RAM through diodes  
20 D1 and D2, respectively. In this configuration, once  
the player is connected to the server, the diode D1 is  
turned on since the operating voltage of the server is  
about 5 V and higher than the voltage of about 4 V  
across the battery E1, and the memory circuit RAM is  
25 operated by the operating voltage from the server side.  
At the same time, the diode D2 on the battery E1 side is  
reversely biased into an off state with the result that  
no reverse current flows from the connector of the

1 server to the battery E1. When the player is pulled off  
from the server, the connector is opened and therefore  
the diode D2 is turned on, thereby supplying the voltage  
across the battery E1 to the memory circuit RAM. By  
5 employing a power supply system of this type, the data  
transfer to the memory circuit RAM can be effected at a  
high speed, while lengthening the battery life of the  
player at the same time.

[0029]

10 Fig. 12 is a schematic diagram showing an  
embodiment of the storage area management system of the  
memory circuit RAM of the player.

According to this embodiment, a digital signal  
is stored and managed by a contents memory and a data  
15 memory. The contents memory can store a maximum of four  
types of digital signals (programs) including contents 1  
to 4, for example. The contents memory may store the  
head address as in the aforementioned embodiment, and  
the contents information in addition to the end address  
20 and ID code designating playback conditions. This  
contents information, though not specifically limited,  
includes character information, so that the program  
contents can be displayed by characters with a liquid  
display unit mounted in the player.

25 Each content of the contents memory and the  
data area of the data memory are arranged as desired in  
such forms as data 2, data 1, data 4 and data 3, for  
example, from the head address side of the data memory

1 in the order of storage. Specifically, digital signals  
are stored in the data memory in the order of  
designation.

[0030]

5 Fig. 13 is a block diagram showing the  
essential parts of an embodiment of the player with the  
contents function added thereto.

The controller CTL includes a switch SW1 for  
designating contents (designating programs) in addition  
10 to the switch SW2 for operation control mentioned above.  
When this switch SW1 is turned on, though not specifi-  
cally limited, a +1 pulse is supplied to the contents  
address counter AC, and the contents memory is accessed.  
The contents information read out of the contents memory  
15 is stored in the contents register whereby such  
characters as title are displayed on the liquid crystal  
display LCD.

[0031]

The head address read out of the contents  
20 memory is set in the address counter of the data memory,  
while the end address and the ID code are loaded in the  
registers REG respectively. The ID code is transmitted  
to the controller CTL and is decoded for automatically  
setting the playback conditioins including the sampling  
25 frequency, the data length, the stereo/monaural mode and  
the like.

The address signal outputted from the address  
counter AC is used for accessing the data memory on the

1 one hand and is supplied to the comparator on the other  
hand. The other input of the comparator CP is supplied  
with the last address loaded in the register REG. As a  
result, when a digital signal (data) corresponding to  
5 the designated contents is completely read, this fact is  
detected by the comparator CP and an end signal is  
inputted to the controller CTL, thereby ending the  
operation of reading a series of digital signals.

[0032]

10 In the above-mentioned indexing function, the  
number of contents may be four or as desired. If such a  
number is the Nth power of 2, however, a binary address  
counter can be conveniently used directly and selection  
is facilitated. Also, in the case where the contents  
15 memory is provided separate from the data memory, they  
are accessible in parallel independently of each other  
thereby to simplify the control of the address counter.  
The above-mentioned contents memory may be course be  
configured by the use of a predetermined storage area of  
20 the data memory.

When the player is connected to the server in  
a digital signal receiving/delivery system mentioned  
above, for example, the server accesses the content  
memory and reads an effective block address. By doing  
25 so, the server can know the vacant area of the memory  
RAM in the player. And when a digital signal to be  
newly received or delivered is designated, a block



1 address is stored in the vacant content while storing a  
digital signal in the vacant area.

[0033]

If the contents are short or there is no  
5 vacant storage capacity available for a digital signal  
received/delivered, the fact is displayed and a digital  
signal already stored is selected. This signal is  
erased and a new digital signal inputted. In the  
process, the digital signal already stored in the player  
10 is also read out, and an address is assigned again not  
to cause any vacant storage capacity in accordance with  
the storage capacity of the new digital signal.

In this way, by managing the storage area of  
the memory RAM of the player on the server side, a  
15 comparatively small storage capacity can be efficiently  
used, and at the same time the control operation on  
player side can be greatly simplified.

[0034]

The effects obtained from the above-mentioned  
20 embodiment are as follows:

(1) The difference between the immediately  
preceding sampling data and an input data is determined,  
and when the difference is larger than the maximum value  
of a compressed code, the particular maximum value is  
25 outputted, while when the difference is smaller than the  
same maximum value, the result of subtraction is  
outputted to output compressed data, thus compressing  
data. In this method, the data such as an acoustic

1 signal having an amplitude or a frequency distribution  
changing comparatively gently with time can be com-  
pressed with high fidelity with a simple configuration  
of subtraction and addition.

5 (2) According to the effect (1) above, a data  
compressor or expander can be realized with a simple  
circuit including a subtractor, an adder, a register and  
a comparator. Also, the power consumption is minimized.

(3) By using a data converter system and circuit  
10 mentioned above, the player for reproducing an acoustic  
signal stored in a memory can be reduced in size and  
weight.

[0035]

Although the present invention has been  
15 described specifically above with reference to  
embodiments, the invention is not limited to these  
embodiments but various modifications thereof are of  
course possible without departing from the spirit of the  
invention. In Fig. 1, for instance, in place of the  
20 configuration for comparing the subtractor output data  
D3 with the maximum value D4 of a compressed data by a  
comparator, an OR gate or the like may be used to form a  
comparator output larger or smaller than the maximum  
value equivalently on the basis of the fact that at  
25 least any one of the most significant bits of the  
subtractor output data D3 is "1". Also, the data D2 of  
the register less the input data D1 may be used as the  
difference data.

1           The input data compressed, instead of the  
output signal of the analog-to-digital converter as  
shown in the embodiment of Fig. 1, may of course be such  
as a digitally-converted data stored in a memory, a  
5 magnetic tape or a compact disk with equal effect. The  
compressed data may be converted into a serial data and  
outputted through a communication channel or the like.

The data converter system and the analog-to-  
digital converter according to the present invention are  
10 widely applicable with circuits and systems handling a  
digital data changing with time.

[0036]

[Effect of the Invention]

The effect obtained by a representative example  
15 of the invention disclosed in this application will be  
briefly explained. Specifically, the difference between  
an immediately preceding sampling data and an input data  
is determined. When the difference is larger than the  
maximum value of a compressed code, the maximum value is  
20 outputted, while it is smaller than the maximum value,  
the subtraction result is outputted to output a  
compressed data, thus attaining data compression. In  
this system, a data such as an acoustic signal in which  
the amplitude or frequency distribution changes in  
25 comparatively gentle way with time can be compressed  
with high fidelity by a simple configuration for  
subtraction and addition. This system can therefore be

1 realized with a simple circuit including a subtractor,  
an adder, a register and a comparator.

[Brief Description of Drawings]

[Fig. 1]

5 A block diagram showing an embodiment of a  
data converter configured of a data conversion system  
according to the present invention.

[Fig. 2]

A diagram showing waveforms for explaining an  
10 example analog/digital converting operation accompanied  
by a data compressing operation according to the  
embodiment in Fig. 1.

[Fig. 3]

A block diagram showing another embodiment of  
15 a data converter configured of a data conversion system  
according to the present invention.

A block diagram showing the essential parts of  
an embodiment of a digital signal receiving/delivery  
system using a data conversion system and a data  
20 converter according to the present invention.

[Fig. 5]

A block diagram showing an input section of  
the terminal device in Fig. 4.

[Fig. 6]

25 A block diagram showing a memory section of  
the terminal device in Fig. 4.

1 [Fig. 7]

A block diagram showing an output section of the terminal device in Fig. 4.

[Fig. 8]

5 A block diagram showing an embodiment of the player used in the digital signal receiving/delivery system described above.

[Fig. 9]

A plan view showing an embodiment of a package  
10 substrate configuring the player.

[Fig. 10]

A side view showing an embodiment of the package substrate as contained in a case.

[Fig. 11]

15 A block diagram showing an embodiment of the power supply system for the player.

[Fig. 12]

A schematic diagram showing an embodiment of the storage area management system of the memory RAM  
20 built in the player.

[Fig. 13]

A block diagram showing the essential parts according to an embodiment of the player having the indexing function of Fig. 12 added thereto.

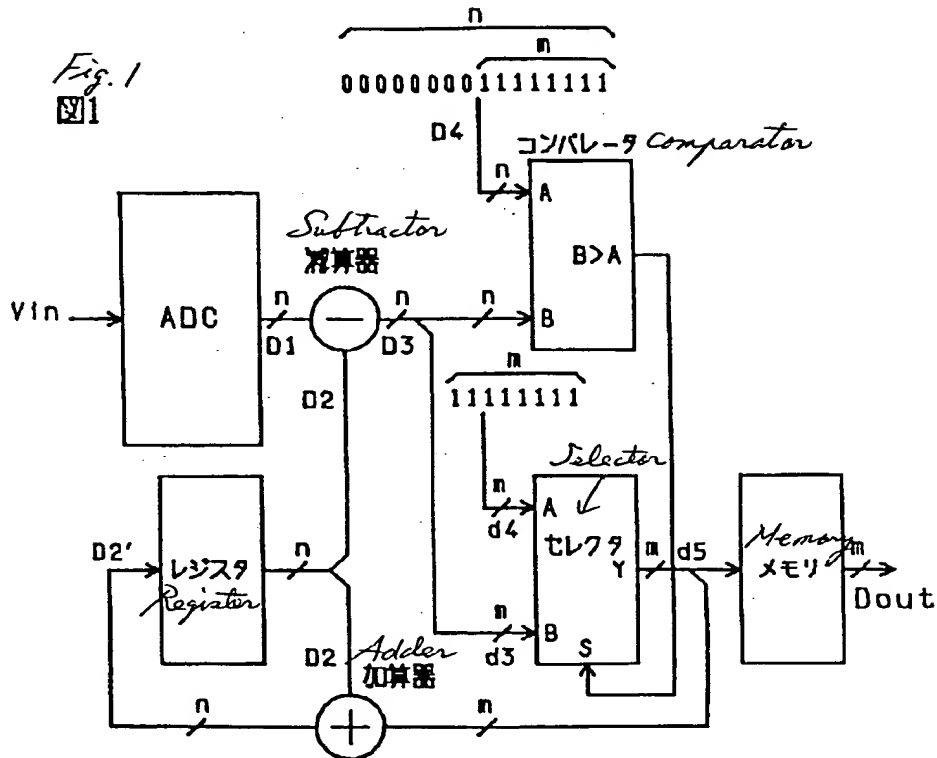
#### [Designation of Reference Characters]

LPF ... Low-pass filter, MPX ... Multiplexer,  
S/H ... Sample & hold circuit, ADC ... Analog/digital

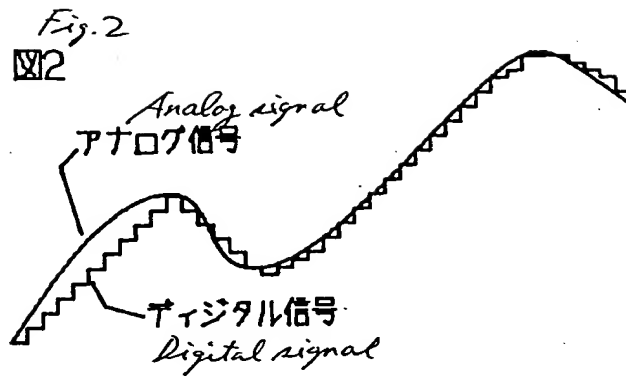
converter, INCT ... Input section controller, NIF ...  
Network interface, CPU ... Microprocessor, ROM ...  
Read-only memory, RAM ... Random access memory (memory),  
HDDC ... Hard disk controller, LCDC ... LCD controller,  
VMEINF ... VME bus interface, HDD ... Hard disk memory,  
LCD ... Liquid crystal display, OUTINF ... Output  
interface, PCTL ... Player controller, BM ... Buffer  
memory, MOCTL ... Monitor controller, MONT ... Monitor,  
DC ... Data converter, AC ... Address counter, CTL ...  
Controller, LSI ... Large scale integration (gate  
array), DAC ... Digital/analog converter, AMP, AMP1,  
AMP2 ... Amplifier, BAT ... Power supply, S2, S3 ...  
Power switch, E1 to E3 ... Battery, SEL ... Selector.

[Title of Document]  
~~[Document name]~~ Drawing  
 【書類名】 図面

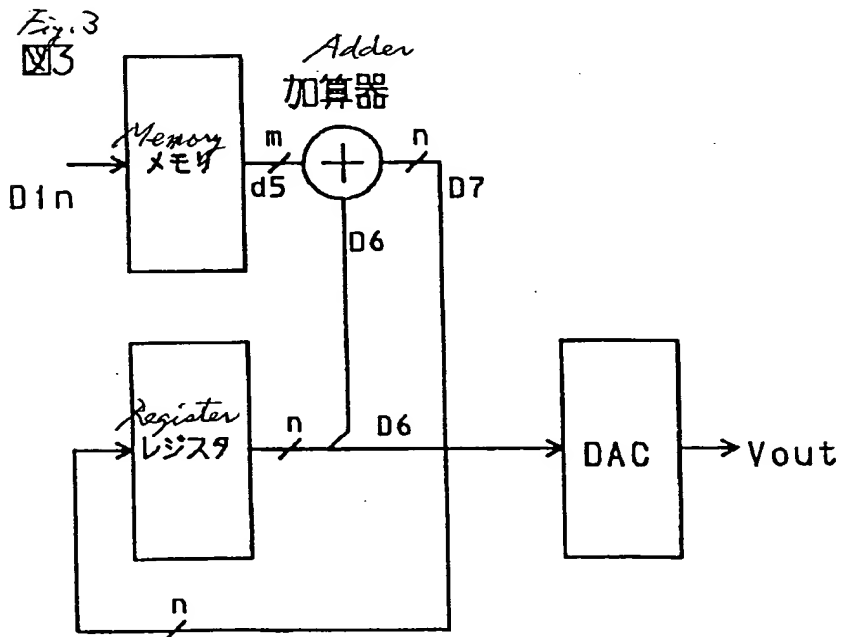
【図1】  
 [Fig.1]



【図 2】  
[Fig.2]



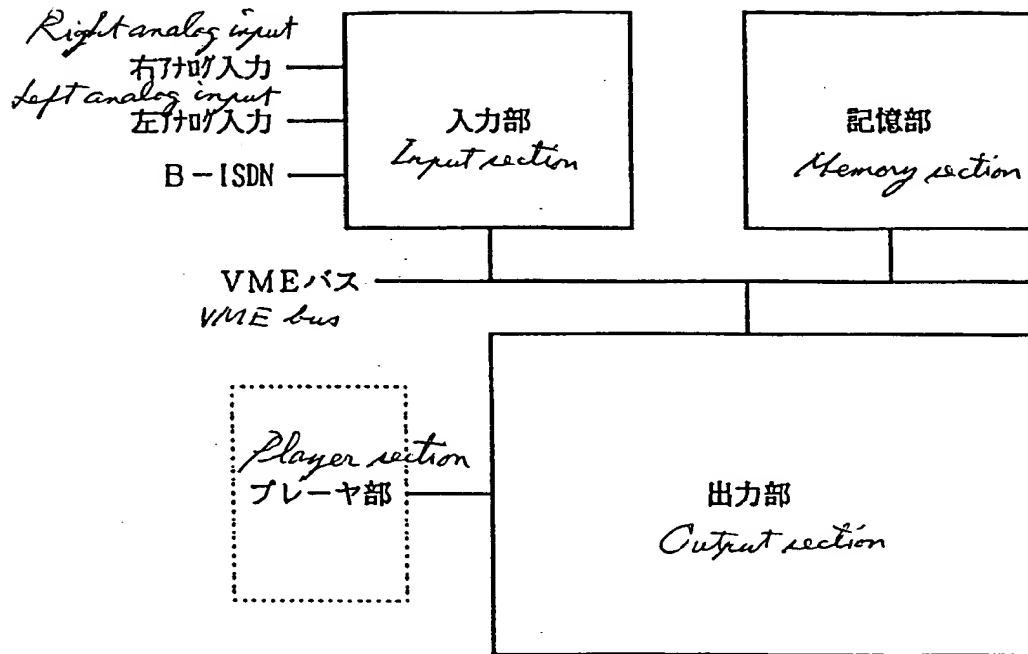
【図 3】  
[Fig.3]



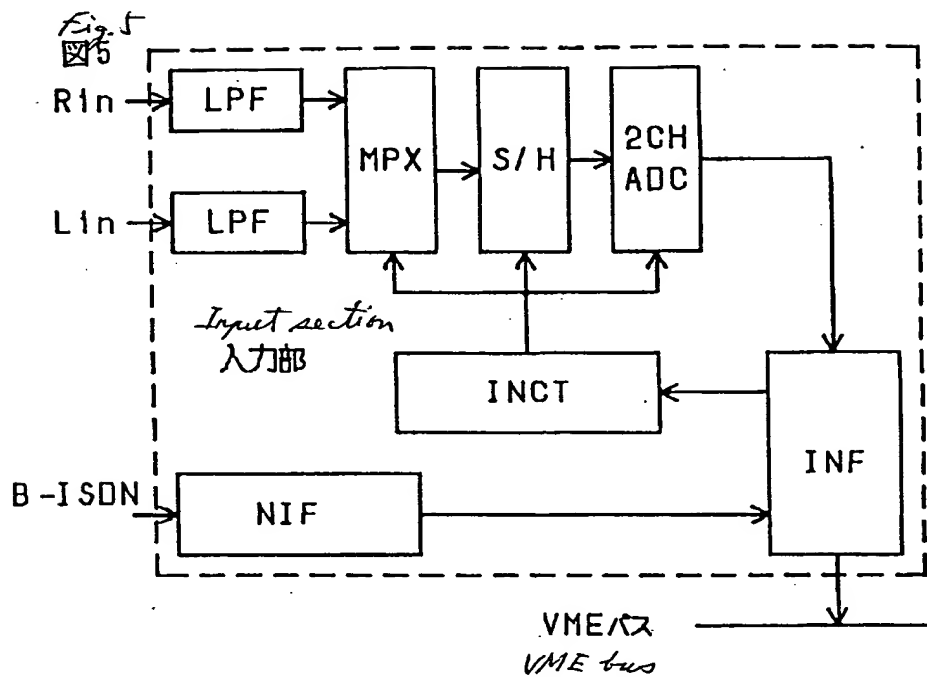


[Fig. 4]  
【図 4】

Fig. 4  
図 4

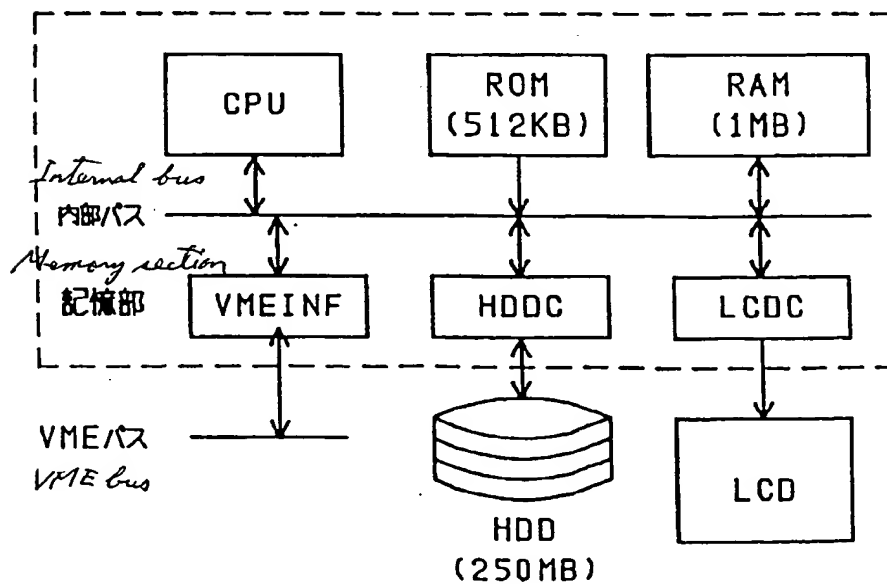


【図5】  
[Fig.5]



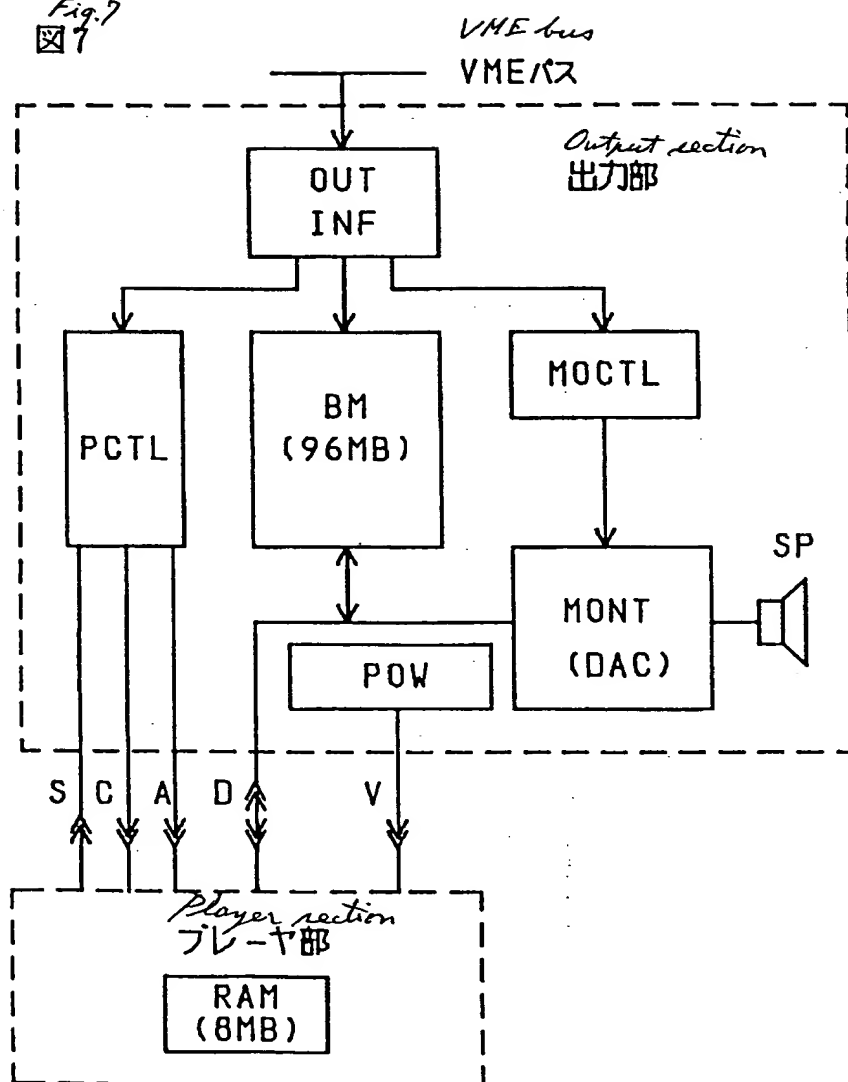
【図6】  
[Fig.6]

図6 Fig.6

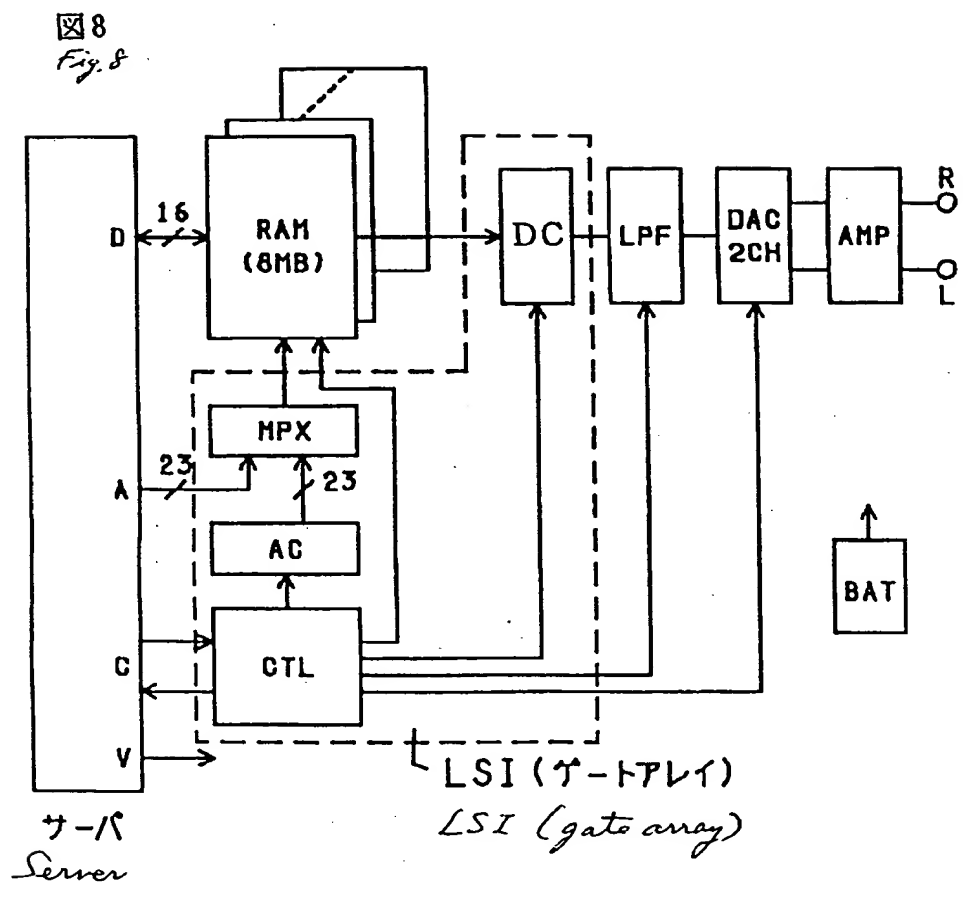


【図 7】  
[Fig. 7]

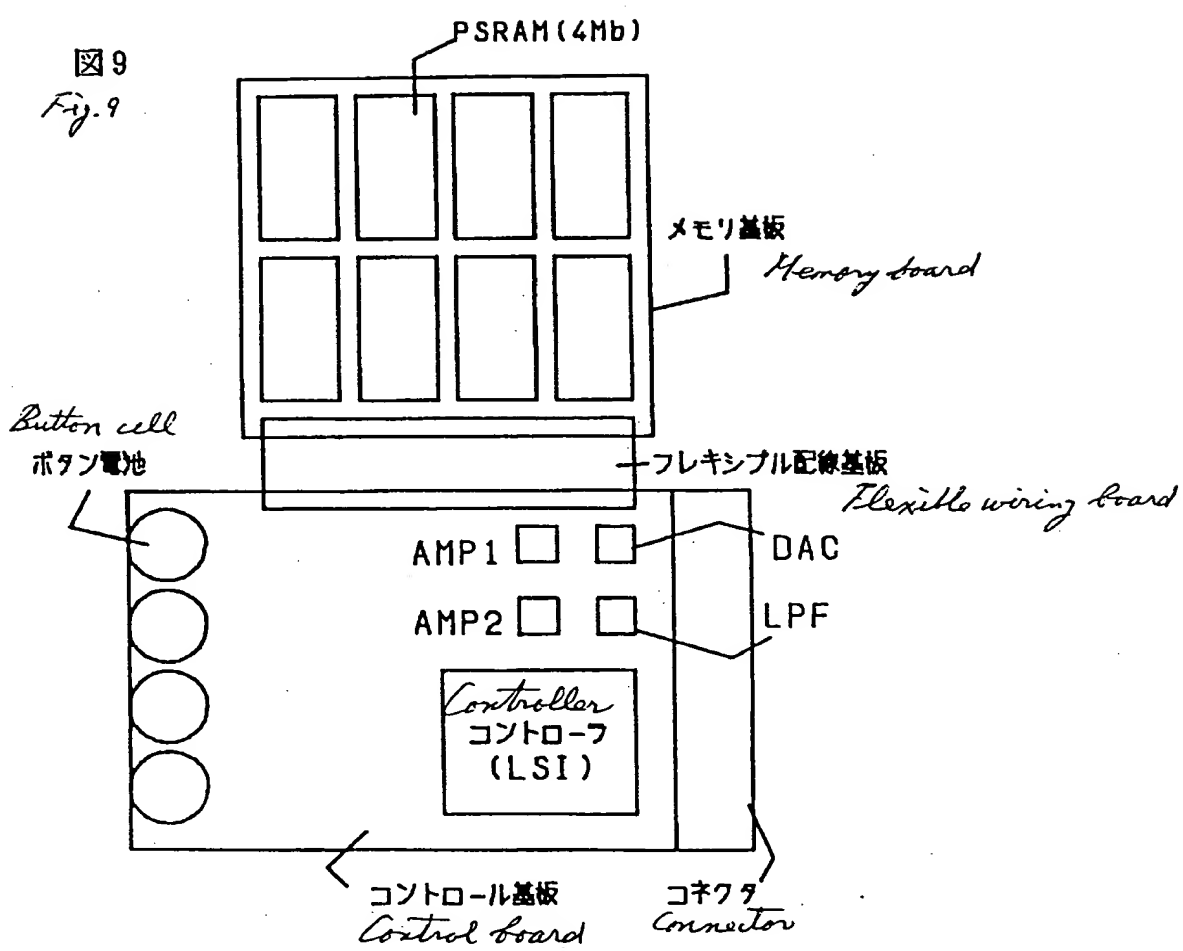
Fig. 7  
図 7



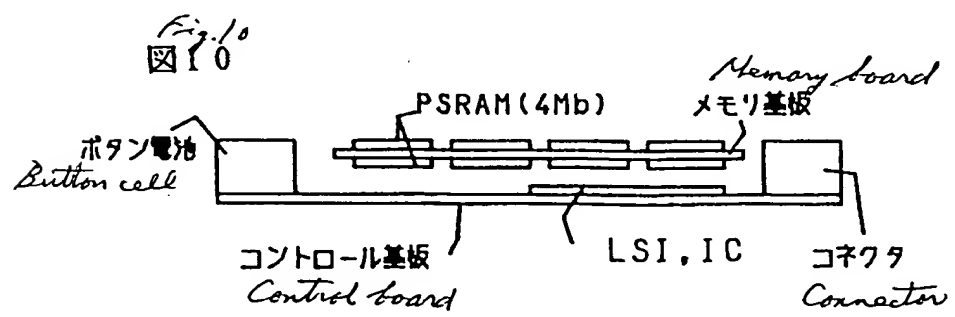
【図 8】  
[Fig. 8]



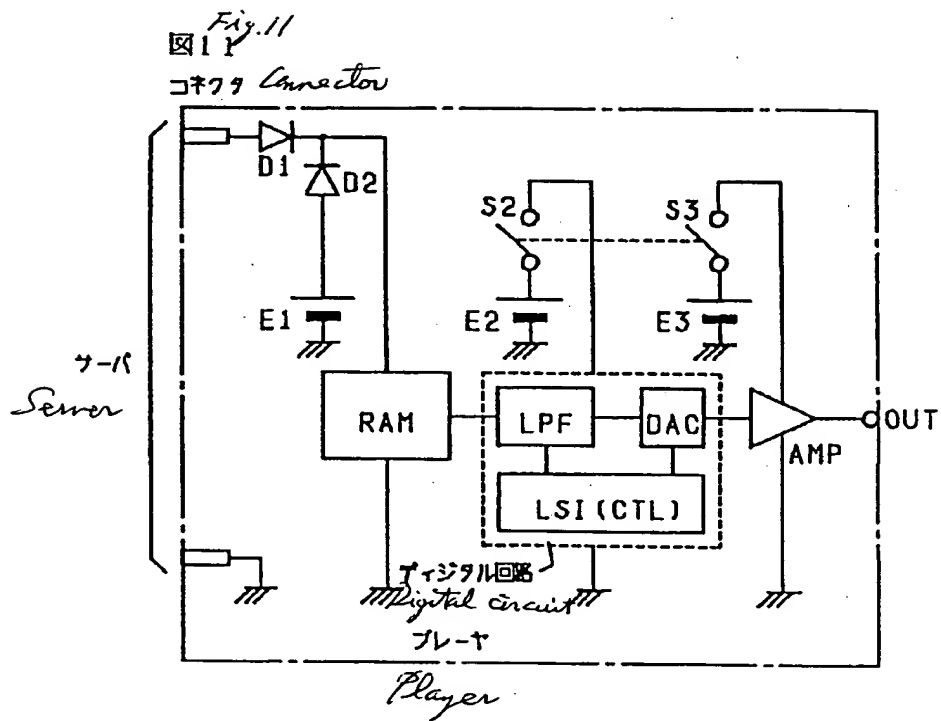
【図9】  
[Fig.9]



【図10】  
[Fig.10]



【図11】  
[Fig. 11]



【図12】

[Fig.12]

Fig.12  
図12

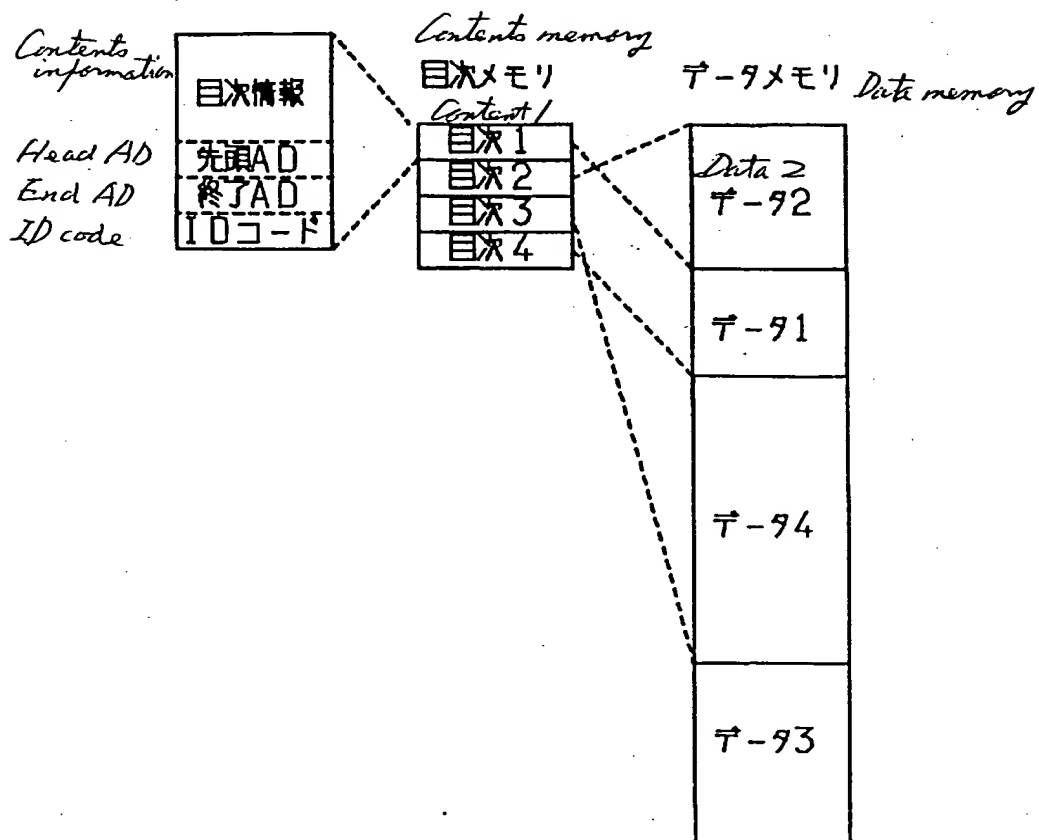
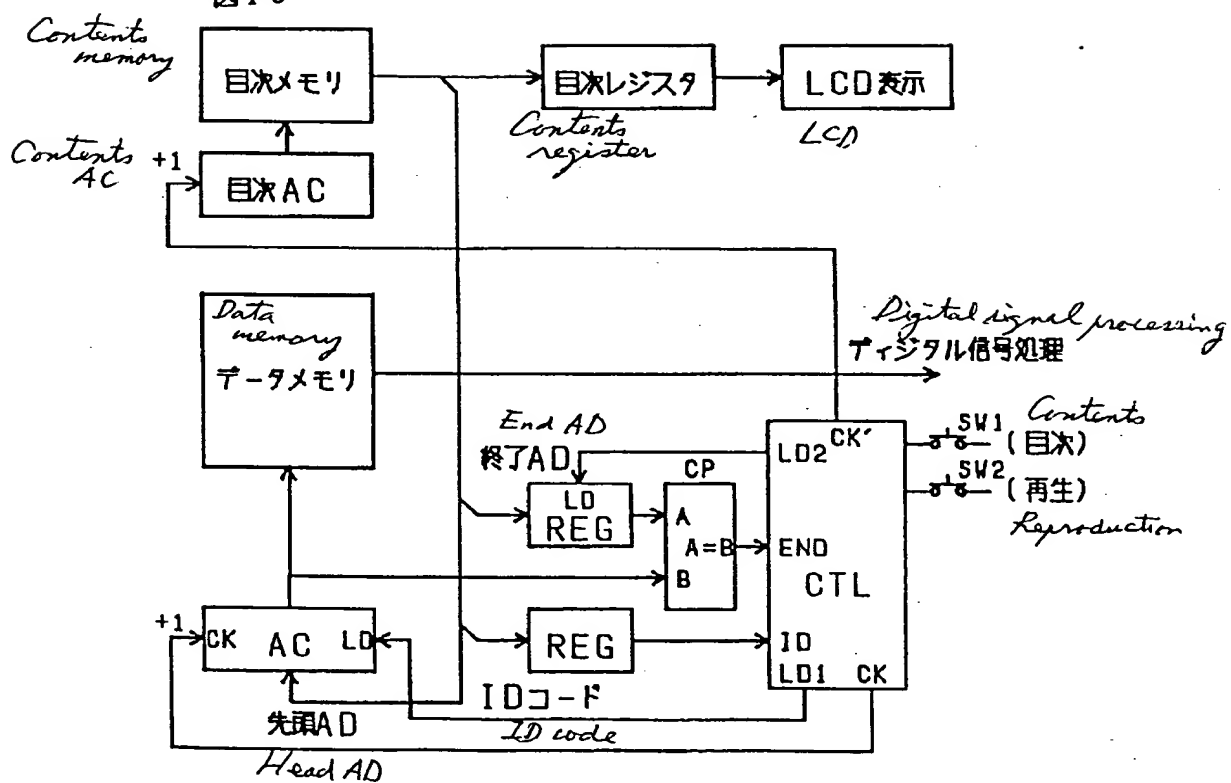


Fig. 13  
图 13





1 [Title of Document]      Abstract

[Summary]

[Object]      To provide a data conversion system and a  
data converter capable of producing a high fidelity with  
5 a simple configuration.

[Configuratin]      The difference between an immediately  
preceding sampling data and an input data is determined.  
When the difference is larger than the maximum value of  
a code to be compressed, the maximum value is outputted,  
10 while when it is smaller, te subtraction result is  
outputted to produce a compressed data. Also, a circuit  
is used in which the difference between the input data  
and an immediately preceding sampling data stored in  
a register is determined, and the subtraction output  
15 thereof is compared with the maximum value of the  
compressed data at a comparator. A selector is  
controlled by the comparison output, so that when  
the subtraction output is larger than the maximum  
value, the particular maximum value is outputted,  
20 while when the subtraction output is smaller than  
the maximum value, the subtraction output is out-  
putted.

[Effect]      Since the amplitude and frequency distri-  
bution of an acoustic signal change in comparatively  
25 gentle manner with time, data compression and extension  
of high fidelity is made possible by the use of the  
data conversion system described above. This data  
compression and extension is realized by a simple

- 1 combination of logic circuits including a subtractor, an adder, a comparator and a register.

[Selected Diagram]      Fig. 1

## SPECIFICATION

## 1 1. Title of the Invention

INFORMATION STORAGE AND REPRODUCTION SYSTEM  
AND METHOD OF STORAGE AND REPRODUCTION

## 2. Scope of Claim for a Patent

5 1. In a recording and reproduction system comprising an input amplifier, an input-side low-pass filter, an AD converter, an IC memory for recording and reproducing a digital data, a DA converter, an output-side low-pass filter, an output amplifier and a control  
10 circuit, an information storage and reproduction system characterized in that a self-diagnosis section is added for skipping a defective address of the IC memory at the time of writing a data into the IC memory.

2. In a method of information storage for  
15 amplifying an analog information at an input amplifier and converting it into a digital data at an AD converter through an input-side low-pass filter, and recording and reproducing it in an IC memory, an information storage and reproduction system including the step of self-  
20 diagnosis having the function of skipping a defective address of the memory at the time of writing a data not the IC memory.

3. In an information recording and reproduction system comprising an input amplifier, an input-side low-

1 pass filter, an AD converter, an IC memory for recording  
and reproducing a digital data, a DA converter, an  
output-side low-pass filter, an output amplifier and a  
control circuit, an information storage and reproduction  
5 system characterized in that a power supply line to  
input-side circuit elements made up of the input  
amplifier, the input-side low-pass filter, the AD  
converter, etc. is separated from a power supply line to  
output-side circuit elements made up of the DA  
10 converter, the output-side low-pass filter, the output  
amplifier, etc.

4. A method of information storage and  
reproduction for amplifying analog information into a  
digital data at an AD converter through an input-side  
15 low-pass filter, recording the digital data in an IC  
memory, converting the digital data from the IC memory  
into analog information at a DA converter at the time of  
reproduction, the information being reproduced by being  
amplified at an output amplifier through an output-side  
20 low-pass filter, wherein a power supply line to input-  
side circuit elements made up of the input amplifier,  
the input-side low-pass filter and the AD converter at  
the time of storage is separated from a power supply  
line to output-side circuit elements made up of the DA  
25 converter, the output-side low-pass filter and the  
output amplifier at the time of reproduction for storage  
and reproduction.

- 1     5.        In a recording and reproduction system for  
analog signals for subjecting a digital data from an IC  
memory to DA conversion at the time of reproduction and  
including an output-side low-pass filter, an output  
5 amplifier and a control circuit, an analog information  
storage system characterized in that an amplifier  
including a nonlinear section with an amplifier factor  
increasing with the analog input signal voltage is  
inserted on the output side of the DA converter.
- 10    6.        In a method of information reproduction  
including the steps of subjecting a digital data from an  
IC memory to DA conversion at the time of reproduction  
and amplifying it at an output amplifier through an  
output-side low-pass filter, a method of information  
15 storage and reproduction characterized by including the  
step of nonlinear conversion suitable for aural sense of  
the human being.
7.        An information storage and reproduction system  
for amplifying analog information at an input amplifier,  
20 converting the information into a digital data at an AD  
converter through an input-side low-pass filter, record-  
ing the digital data in an IC memory, and converting the  
digital data from the IC memory into analog information  
at a DA converter at the time of reproduction, the  
25 analog information being amplifier at an output  
amplifier through an output-side low-pass filter for  
reproduction, characterized in that the information is  
dubbed from a first information storage and reproduction

1 system into at least a second information storage and  
reproduction system at the speed of ten times higher  
than the time required for reproduction.

8. A method of information storage and reproduc-  
5 tion system for amplifying analog information at an  
input amplifier, converting the analog information into a  
digital data at an AD converter through an input-side  
low-pass filter, recording the digital data in an IC  
memory, and at the time of reproduction, converting the  
10 digital data from the IC memory into analog information  
at a DA converter and reproducing by amplifying the  
information at an output amplifier through an output-  
side low-pass filter, characterized by including the  
step of re-storing or re-reading the information within  
15 a time less than at least one-tenth the time required  
for reproduction.

9. A method of information storage for amplifying  
analog information at an input amplifier and storing the  
AD-converted digital signal in a dynamic-type IC memory  
20 requiring refreshing operation through an input-side  
low-pass filter, characterized by including the step of  
erasing the data stored in the IC memory collectively by  
stopping the refreshing operation of the IC memory.

10. An information storage and reproduction system  
25 wherein a discrimination mark, indicating the type  
relating to the attribute of an IC memory is attached on  
a case accommodating the IC memory, characterized by  
having decision means for identifying the discrimination

1 mark on the side of the system carrying the case for  
accommodating the IC memory.

11. An information storage and reproduction system  
as described in Claim 10, characterized in that at least  
5 a part of the means for carrying the case accommodating  
the IC memory is transparent.

### 3. Detailed Description of the Invention [Industrial Field of Utilization]

The present invention relates to an analog  
10 information storage system of full-solid type and a  
method thereof in which analog information such as  
voice, image, temperature and pressure due to a full-  
solid device is capable of being recorded into and  
reproduced from an IC memory in digital fashion.

#### 15 [Prior Art]

Conventionally, what is called an audio tape  
recorder is commonplace as a system for recording/  
reproducing the voice or the like. In recent years,  
however, a method has been widely extended in which  
20 analog information is digitized temporarily and  
digitally recorded in an optical disk or magnetic tape,  
followed by being restored into analog information such  
as a voice at the time of reproduction. As disclosed in  
JP-A-62-187898, for example, digital information is  
25 stored in an IC memory, and at the time of reproduction,  
information from the IC memory is converted into analog

1 from digital information, and through an amplifier, the  
voice is reproduced by speaker or earphone.

[Problem that the Invention is to Solve]

The above-mentioned prior art fails to take  
5 into account a method or system for storage and re-  
production taking full advantage of the features of an  
IC memory, thus posing the problem in terms of  
efficiency, size reduction, improves speed, higher  
reliability and lower power consumption of recording and  
10 reproduction.

An object of the present invention is to use  
an IC memory as a recording/reproduction medium and to  
minimize the scale of the peripheral circuits of a  
memory.

15 Another object of the present invention is to  
attain the possibility of utilizing even an IC memory  
having a defective cell.

Still another object of the present invention  
is to minimize power consumption even at the time of  
20 recording or reproduction as well as at the time of  
standby (when only the contents of a memory are held).

A further object of the present invention is  
to provide a conversion function conforming to the aural  
sense of the human being against audio information.

25 A still further object of the present  
invention is to provide the function of a high-speed  
dubbing of analog information for transferring the  
contents stored in an IC memory outside at high speed.



1           Another object of the present invention is to  
erase the contents of an IC memory collectively in an  
instant.

          Still another object of the present invention  
5 is to prevent the circuit voltage from dropping even  
against an instantaneous large power consumption of a  
battery.

          A further object of the present invention is  
to improve the yield by using the function of a DA  
10 converter also as that of an AD converter at the same  
time and thus reducing the chip area.

          A still further object of the present  
invention is to provide a display unit in which a block  
is designated selectively, indicating the search  
15 operation, when there are a plurality of contents to be  
recorded or reproduced.

[Means for Solving the Problem]

          In order to achieve the above-mentioned  
objects, a digital data section (if necessary, including  
20 AD or DA conversion section) including an IC memory is  
formed as a one-chip integrator circuit (IC).

          In order to achieve the other objects  
mentioned above, a self-diagnosis circuit is added for  
performing the recording operation while deciding  
25 whether the recording is possible in an IC memory.

          In order to achieve the other objects  
mentioned above, a power supply line is divided into  
three systems including a circuit section used only at

1 the time of recoding, a circuit section used only at the  
time of reproduction and a circuit section normally  
used, and the former two systems of power supply line  
are provided with a control switch of a transistor or  
5 the like respectively.

In order to achieve the other objects  
mentioned above, a nonlinear amplifier with the  
amplification factor thereof changed in accordance with  
input signal level is inserted in the rear stage of a DA  
10 converter.

In order to achieve the other objects  
mentioned above, a data selector circuit having an  
output data of an AD converter and an input digital data  
from outside applied thereto is inserted in the front  
15 stage of an IC memory.

In order to achieve the other objects  
mentioned above, an erase switch is provided, together  
with two monostable multivibrators and analog signal  
adder circuits for controlling a circuit for writing "0"  
20 into an IC memory and a pulse generator, so that the  
signal of the pulse generator is added to the analog  
output signal from a DA converter.

In order to achieve the other objects  
mentioned above, a resistor (connected in series) and a  
25 large-capacity capacitor (connected in parallel) are  
added to a button-type lithium cell, so that the circuit  
power is obtained not directly from the lithium cell but  
from the large-capacity capacitor.

1           In order to achieve the other objects  
mentioned above, a data selector circuit, a counter, an  
analog comparator, etc. are disposed in the input side  
of the DA converter, so that the data from the IC memory  
5 is selected at the time of reproduction and the output  
data from the counter at the time of recording, while  
the output signal and the input signal of the DA  
converter are compared at an analog comparator, thus  
making up an AD converter.

10           In order to achieve the objects mentioned  
above, there are provided a memory for recording the  
contents of an address counter, a circuit for reloading  
(setting) the contents of the memory in the address  
counter, and a switch and a display unit for selecting  
15 an intended block.

[Operation]

A digital data system in the form of one-chip  
integrated circuit improves the reliability of a signal  
transmission system, etc. greatly. As a result, the  
20 peripheral circuits of a memory including an error  
correction circuit are eliminated, thereby reducing  
power consumption.

Also, a self-diagnosis circuit inserted in the  
front stage of a memory always decides whether an  
25 intended data can be recorded, and if the decision is  
that the intended data is an address that cannot be  
recorded, operates to skip the particular address. As a  
result, even an IC memory having a somewhat defective

1 cell is usable, thereby greatly contributing to a  
reduced cost.

Further, a transistor switch inserted in the  
recording circuit system and the reproduction circuit  
5 system operates in such a manner as to conduct only when  
each of the systems requires electric power. As a  
result, power is not supplied to the reproduction side  
at the time of recording, to the recording side at the  
time of reproduction, and to the recording and reproduc-  
10 tion sides at the time of standby, thereby greatly  
reducing the average power consumption.

Furthermore, a nonlinear amplifier inserted in  
the rear stage of a DA converter operates in such a  
manner as to produce a smaller level of signal when an  
15 input signal level is small, and a larger level of  
signal when an input signal level is large. As a  
result, the quantization noise (a noise generated by a  
change of a bit smallest in weight) of an AD converter  
is reduced when the input signal level is small, while  
20 when the input signal level is large, the particular  
magnitude is emphasized. Therefore, even in the  
quantization of eight bits, for example, the noise level  
and dynamic range equivalent to more than ten bits can  
be secured.

25 Also, a data selector inserted in the rear  
side of the AD converter operates in such a manner as to  
switch between an output data of the AD converter and an  
external digital data applied to the data line of an IC

1 memory. As a result, the digitized analog information  
transferred from an external source in the form of a  
clock frequency one hundred times larger in magnitude,  
for example, is stored in the IC memory in a time one  
5 hundredth shorter.

Further, two monostable multivibrators control  
pulse generators of different frequencies. These  
operate in such a manner as to produce signal sounds of  
different frequencies from the earphone and thus prevent  
10 the erroneous erasure due to an operation error in order  
to confirm with the user whether or not the erasure is  
really permitted.

Further, a large-capacity capacitor connected  
in parallel to a button-type lithium cell through a  
15 resistor is adapted not to supply the circuit power  
directly from the button-type lithium cell but to supply  
the power stored in the capacitor temporarily and  
operates in such a manner as to maintain a constant  
voltage by absorbing pulse-like variations of the load.

20 Further, a DA converter and the peripheral  
circuits thereof having the function also of an AD  
converter act as a DA converter or an AD converter as  
required (shares the two functions). Therefore, the  
chip area is reduced for an improved yield, while at the  
25 same time eliminating the need of an AD converter  
technically difficult to produce, thus permitting a  
lower IC cost.

1           Further, a memory for storing the contents of  
an address counter or loading (setting) the stored  
address information again in the address counter and the  
peripheral circuits thereof operate in such a manner as  
5 to determine the head address of a block or set the head  
address for immediate reproduction of the desired block,  
facilitating the search in order to prevent a vacant  
space from being generated in the memory storing the  
input information (in order to improve the operating  
10 efficiency of the memory) when there are a plurality of  
contents to be recorded or reproduced. Also, the addi-  
tion of a display unit indicating the search operation  
realizes a system very convenient to use.

[Embodiments]

15           An embodiment of the present invention will be  
described below with reference to the drawings.

Fig. 1 is a functional block diagram showing a  
first embodiment of the present invention, and  
represents a case in which all devices including a cell  
20 are incorporated in a headphone with microphone. This  
embodiment comprises an input amplifier 1 for amplifying  
the output of the microphone (a capacitor microphone is  
used in the embodiment under consideration, though not  
shown in the drawings) and the line output of audio  
25 equipment to the operating level of an AD converter, an  
input-side low-pass filter 2 for blocking the frequency  
components of more than one half of a sampling frequency  
in quantization, an AD converter 3 for quantizing (into

1 a digital code of 8 bits according to the present  
embodiment) an input analog signal, an IC memory 4 for  
recording/reproducing a digital code data, a DA  
converter 5 for restoring the reproduced digital code  
5 data into analog information, an output-side low-pass  
filter 6 for eliminating the high-frequency noises  
generated at the time of restoring the analog informa-  
tion from the digital code data, an output amplifier 7  
for driving the earphone or speaker (a crystal earphone  
10 and a ceramic speaker are used in the embodiment under  
consideration, though not shown in the drawings), a  
control circuit 8 for controlling the write or read  
operation for the IC memory, a button-type lithium  
primary dry cell 13 and operating switches 9, 10, 11,  
15 12. First, audio information converted not a voltage  
signal by microphone is amplified to a maximum amplitude  
of 4 volts by the input amplifier 1, and through the  
low-pass filter 2 for attenuating the frequencies of  
more than 2 KMz, if increased ten times, by a factor of  
20 the thousands, is applied to the 8-bit AD converter 3.  
The AD converter 3 is energized for converting operation  
with a sample clock of eight KHz, and the audio informa-  
tion converted into a digital data is written into the  
IC memory 4. Such a recording operation as this (opera-  
25 tion for writing into the memory) is performed in such a  
manner that when a PLAY switch 9 is depressed while  
depressing a REC switch 10, the control circuit 8  
recognizes a starting command for the recording opera-

tion, and by reducing a WF output to low level, a transistor Q2 is turned on through a resistors R2, thus supplying the electric power from the lithium cell 13 to the circuit units of the recording system, that is, the input amplifier 1, the input-side low-pass filter 2 and the AD converter 3. Subsequently, a sampling clock is applied to the AD converter, while at the same time generating a write strobe signal and an address data for the IC memory (this address is incremented at the trailing edge of the write strobe signal). For reproducing the audio information accumulated in the IC memory, on the other hand, only the PLAY switch 9 is depressed whereby the control circuit 8 recognizes a reproduction operation command. The RF flag is thus reduced to low level, so that the transistor Q1 is turned on through the resistor R1 thereby to supply power to the reproduction circuit system. Subsequently, the address data is supplied to the IC memory 4, and a strobe read out is outputted to the DA converter 5, with the address incremented at the trailing edge of the strobe read out as above. As a result, the digitized audio data read out of the IC memory 4 in orderly manner is returned to a stepped analog signal at the DA converter 5, and processed into a smooth waveform by the function of the outer-side low-pass filter 6. The earphone or speaker is energized through the output amplifier 7 for restoring the signal to audio one. By the way, the frame 14 defined by the one-dot chain represents the AD



1 converter 3, the IC memory 4, the DA converter 5 and the  
control circuit 8 integrated into a one-chip integrated  
circuit. The frame 15 defined by a dotted line  
represents a base substrate for forming a hybrid IC  
5 (According to the embodiment under consideration, an  
attempt was made in vain to integrate the one-chip  
integrated circuit with the base substrate). Also, the  
frame 16 defined by a two-dot chain represents a section  
made into an IC or hybrid IC except for the memory IC  
10 portion with the intention of using a standardized  
large-capacity memory card. As a result, it becomes  
possible to mount and demount the memory section (medium  
section), the information transmission is facilitated by  
delivery of the memory card as in the case of floppy  
15 disk, and in addition, the compatibility with a ROM card  
is secured. Thus information (software) can be produced  
in great volume at low cost.

In similar fashion, exactly the same effect  
was obtained by trying a system in which the devices  
20 including the AD converter 3, the DA converter 5 and the  
control circuit 8 except for the IC memory 4 in the  
frame defined by the one-dot chain 14 are formed in a  
one-chip integrated circuit, while at the same time  
forming an IC or hybrid IC including the input- and  
25 output-side low-pass filters 6 and 7, the input  
amplifier 1, the output amplifier 7, etc. thus making  
the memory card replaceable.

1           By the way, if the recording or reproducing  
operation is to be ended, the STOP switch 11 is  
depressed, with the PAUS switch 12 depressed once. The  
operation is then suspended. At another press of the  
5 PAUS switch 12, the recording or reproducing operation  
is restarted.

          According to the present embodiment, the  
system is reduced to such an extent that all the  
principal circuits including the battery cell are  
10 packaged in the ear portion of the headphone with  
microphone used by the telephone operator or the like.  
At the same time, power consumption is about 50  
microwatts (a current of 8 microamperes under a 6-volt  
voltage) at the time of standby, and about 50 millwatts  
15 (a current of 8 milliamperes under a voltage of 6 volts)  
at the time of recording in actual measurements, thus  
realizing a compact system extremely small in power  
consumption. This indicates that even when a button-  
type lithium battery cell of small capacity (190  
20 milliampere hours) is used as a power supply, it is  
possible to perform the reproducing operation for more  
than 30 hours continuously or to reproduce a voice  
recorded and left to stand for 540 days. These values  
have still room for remarkable improvement with the  
25 technical progress of the integrated circuit and the  
battery cell, and it may be possible to realize a system  
which is capable of holding the record for several years  
or performing the recording/reproducing operation for

1 more than several hundred hours or further reducing the  
size and weight. By the way, by providing an expansion  
connector terminal in the input-output signal pin of the  
internal IC memory (4 of Fig. 1) as an option, an  
5 external memory may be used, thereby making possible the  
recording or reproduction for long hours. If a very  
large scale integration memory system of about 2 giga  
bits ( $2 \times 9$ th power of 10 bits) with a changing  
frequency of about 12 to 16 bits and 15 to 45 kHz for  
10 the AD and DA conversion is used, for example, it is  
possible to record a high-quality music for one hour or  
two.

Fig. 2 is a block diagram showing a second  
embodiment. The circuit configuration of the entire  
15 system is identical to that shown in Fig. 1 of the first  
embodiment, except that a self-diagnosis circuit section  
is added to the peripheral parts of the IC memory 4.  
This embodiment is configured of a data selector 31 for  
selecting the input data of a recording data memory,  
20 i.e., the output data of an AD converter (3 of Fig. 1)  
and tow types of data patterns "AA" and "55" for memory  
test, a ternary counter 32 for giving a selection signal  
to the selector 31, a tri-state buffer 21 for connecting  
the output of the data selector 31, i.e., the data to be  
25 recorded to the data line of the IC memory, an OR  
circuit 22, a pulse delay circuit 23, an address counter  
24, a digital comparator 25, an AND circuit 26 and a  
FIFO memory 27. Input-output signals to the circuit

1 section include an output data from the AD converter  
(memory input data), an input signal to the DA converter  
(5 of Fig. 1) (memory output data), a write strobe  
signal (WE) into the IC memory from the control circuit  
5 section (8 of Fig. 1), a RUN signal (RUN) indicating the  
system in recording or reproducing operation and two  
types of test pattern data "AA" and "55". The skip  
address output and the reproduction clock input are  
signals for reading by skipping a defective portion  
10 (defective address) of the IC memory at the time of  
reproducing operation. Immediately after the recording  
data (memory input data) has undergone a change, the  
strobe signal (WE) is applied with a pulse width of 100  
nanoseconds (repetitive frequency of 8 kHz), and  
15 through the OR circuit 28, clears the ternary counter  
32. Further through the OR circuit 3 and the NOR  
circuit 22, the signal is connected to the control  
terminal of the tri-state buffer 21 and the WE (write  
enable) of the IC memory 4. The output of the tri-state  
20 buffer 21 is in the state of high impedance when the  
control terminal is at high level, and only when the  
control terminal becomes low in level, the input state  
of the device is reflected in the output side. The data  
line of one of the IC memories 4 (DIO) is adapted to  
25 produce the contents of a designated address when the WE  
terminal is at high level, while when the WE terminals  
becomes low in level, the DIO terminal switches to a  
state capable of data input thereby to write the data at

1 the DIO terminal into the designated address. If the  
data at the input and output sides of the tri-state  
buffer 21 are coincident with each other immediately  
after the WE pulse signal has returned to high level  
5 (more exactly, after the lapse of 50 nanoseconds of  
access time of the IC memory), therefore, it indicates  
that a data has been normally written into the IC memory  
4. If the data fail to coincide with each other, on the  
other hand, it is indicative of the fact that it was  
10 impossible to write into the memory 4. In order to make  
this decision, a digital comparator 25 is provided, and  
the Y output of the comparator 25 is logically con-  
figured of no-coincidence outputs in such a manner as to  
take a high level when the contents of A and B inputs  
15 fail to coincide with each other. The Y output of the  
comparator is applied as one of the inputs to the AND  
circuit 26. Further, the output of the OR circuit 22 is  
applied to the pulse delay circuit 23 with inverter  
function, and becomes a WE' pulse delayed by about 200  
20 nanoseconds due to the delay circuit 23, thus making up  
the other input of the AND circuit 26. In the process,  
if the no-coincidence output is at low level, i.e., if  
information is normally written into the memory 4,  
nothing is outputted at the output of the AND circuit  
25 26. At the time of inputting of the WE pulse, the  
ternary counter 32 is reset (although a pulse is also  
inputted to the clock input CP, priority is given to the  
clearing operation). Therefore, both the QA and QB

1 outputs of the counter 32 are at low level and the data  
selector 31 selects the pattern "AA" (expressed in  
sexadecimal notation. Given as 10101010 from the 7-th  
power bit side of 2 in binary notation). Therefore, the  
5 data written normally into the IC memory forms the first  
test pattern. Since the QB output of the ternary  
counter 32 (0th-power bit of 2) is at low level, the  
particular output is high in level at the inverter 29,  
so that the AND circuit 30 passes the WE', and counts up  
10 the ternary counter 32 through the OR circuit 33, so  
that the data selector 31 selects the test pattern "55"  
(expressed in sexadecimal notation. In binary notation,  
01010101 from the 7th-power bit side of 2), and at the  
same time the output of the OR circuit 33 becomes an  
15 input to the NOR circuit 22, thus functioning as a write  
pulse to the memory. After that, when the test pattern  
"55" or the recording data (memory input data) is  
written normally, the AND circuit 30 is inhibited (since  
the QB output of the ternary counter 32 rises to high  
20 level), with the result that the above-mentioned loop is  
opened. Instead, the WE' pulse passes through the AND  
circuit 34, and the address counter 24 is counted up,  
waiting for the next write pulse (WE) from the control  
circuit. Also, in the case where the Y output (no-  
25 coincidence output) of the comparator is at high level,  
that is, when a data is not normally written into the IC  
memory 4, the WE' pulse passes through the AND circuit  
26. The contents of the address counter 24 prevailing

1 at that time are written into the FIFO memory 27. At  
the same time, since the signal is applied to the NOR  
circuit 22 and the OR circuit 28, the same operation as  
when the WE pulse is applied is repeated once again. By  
5 the way, this repetitive operation is continued until a  
data is normally written into the memory 4 (The time  
required for this repetitive operation is about 300  
nanoseconds and the WE input period is about 125 micro-  
seconds, so that the number of repetitions actually  
10 allowed is about 400 in the case of repetition with the  
generation of an error at the time of the first pattern  
check, i.e., at the time of writing the "AA" pattern,  
while it is about 200 in the case of repetitions with  
the error generation at the time of the second pattern  
15 check, that is, at the time of writing the pattern  
"55").

According to the present embodiment, it is  
possible to use IC memory chips which otherwise might be  
discarded as a result of inspection due to the defect of  
20 a memory cell of only several bits of all the large-  
capacity memory cells of mega bit class, say, 4 or 16  
mega bits, with the result that a very inexpensive  
system is provided. The concept described here is based  
on the utilization of defective bits by inspection  
25 before writing and the use of the result thereof, and by  
use of this concept, various modifications and applica-  
tions are of course possible. When "1" is written,

1 assume that a defective bit fixed to "1" is detected as  
a result of inspection. It may be used directly as "1".

By the way, by fixing the operation of the  
data selector in Fig. 2 (the QA output of the ternary  
5 counter 32 is fixed to low level, and the QB output  
thereof to high level), it is possible to configure a  
simple self-diagnosis circuit according to a method of  
checking while writing into an IC memory using only the  
write data.

10 Fig. 3 is a diagram showing a third embodi-  
ment. (a) of Fig. 3 shows a case in which a nonlinear  
circuit 35 is inserted between the DA converter 5 and  
the low-pass filter 6 in Fig. 1 shown in the first  
embodiment, with the characteristic of the output signal  
15 36 of the circuit 35 shown in (b) of the same diagram.  
In (b) of the diagram, the input voltage represents the  
output voltage of the DA converter 5 having an amplitude  
level limited by the circuit voltage (source voltage).

The present embodiment functions rather as an  
20 attenuation amplifier when supplied with a small signal  
as an input, so that a cacophonous quantization noise (a  
noise unavoidably generated by a change in the lightest  
bit of AD conversion). Also, since the system operates  
as an amplifier having a higher gain, the dynamic range  
25 is increased remarkably.

Fig. 4 shows a fourth embodiment, the general  
configuration of which is identical to that of the first  
embodiment shown in Fig. 1. The fourth embodiment



1 represents a case of high-speed data transfer by photo-  
coupling and includes, in addition to the configuration  
of Fig. 1, a photo-sensor 41, an I-V amplifier 42, a PLL  
transmitter circuit 43, a serial-parallel conversion  
5 shift register 44, a mode switch 47 and a data selector  
46. Normally (when the mode switch 47 is set to INT  
side), an analog signal such as an audio signal is  
digitized by the AD converter 3, and together with the  
write strobe signal WE produced from the control circuit  
10 (8 of Fig. 1), is passed through the data selector 46  
and written into the IC memory 4. In serial external  
mode (with the mode switch 47 set to EXT serial side),  
the B input is selected of the data selector 46 to form  
a Y output. The external data supplied as an optical  
15 pulse train (2 bits of start bit indicating the "1" and  
"0" states are added to the head of the unit write data  
train) is thus written into the IC memory 4. Speci-  
fically, a light-modulated pulse train is converted into  
a current signal at a photo sensor 41, shaped in  
20 waveform as a voltage signal at the I-V amplifier 42,  
and is applied to the PLL transmitter circuit 43 for  
extracting the clock components from the shaped pulse  
train, while at the same time being applied to the  
series signal input terminal D of the serial-parallel  
25 conversion shift register 44. The clock signal (8 MHz  
in frequency according to the present embodiment)  
extracted at the PLL transmitter circuit 43 forms a  
shift clock for the shift register 44, and at the same

1 time a count clock for the counter of one n-th (n: The  
number of quantization bits plus 2, which is ten  
according to the present embodiment). The output  
signal (800 kHz according to the present embodiment) of  
5 the counter 45 makes up a write strobe signal for the IC  
memory 4 in place of the write strobe signal WE from the  
control circuit.

By the way, in parallel external mode (with  
the mode switch 47 turned to the EXT parallel side), the  
10 B input of the data selector 49 is selected. The 8-bit  
parallel data is passed through the data selector 46  
from the input buffer 48 and written into the IC  
memory 4.

Fig. 5 is a diagram showing a data transmitter  
15 section according to a fourth embodiment. An 8-bit  
parallel data is produced from the buffer 50 as a data  
of the IC memory 4. Also, the light-modulated pulse has  
the data of the IC memory 4 converted into a serial  
signal at a serial-parallel conversion shift register  
20 37, and 2 bits of start bit representing the states of  
"1" and "0" are added to the head of the data train at a  
start bit adder circuit 38, and the laser diode 40 is  
driven at the V-I amplifier 39 and produced as a light  
pulse train.

25 According to the present embodiment,  
information such as an audio signal is capable of being  
received at high speed wirelessly by photo-coupling. In  
the present embodiment, for instance, an audio data of

1 five minutes could be received in three seconds. Also,  
in the case where the frequency of the clock signal is  
set to 800 kHz with the intention of reducing the  
current consumed at the time of high speed transfer, a  
5 satisfactory result was obtained although some time  
length is required.

The basic concept of the present operation  
lies in that taking note of the operating speed of a  
digital memory higher than the analog signal processed,  
10 the contents of a memory are transferred directly by a  
digital signal at high speed. Many applications of  
operation are of course possible in the framework of  
this concept. The function of transferring the contents  
stored in the IC memory in the system, such as a circuit  
15 for high-speed data transfer to the memory section of a  
system similar to the present system (a system ex-  
clusively used for reproduction comprising only a read  
section), may be provided. Exactly the same result is  
obtained by connecting to a data transfer source  
20 directly by cable instead of by optical coupling system,  
for example. Also, the function of electric wave or  
magnetism may be used. Further, in a system for  
transmitting or receiving an 8-bit parallel data,  
although the circuit at the transmitting or receiving  
25 end is simplified and the number of connector pins is  
increased, the transfer time is shortened further by one  
digit, with the result that an audio data of five

1 minutes could be transmitted and received in 0.3  
seconds.

Further, according to the present embodiment,  
transfer is started at the first address (zero address)  
5 of the IC memory 4, and at the time point of overflowing  
of the address counter (the address counter 24 of Fig.  
2, for instance), the transfer is terminated. By  
providing the ID information at the head portion of the  
transfer data train, however, it has been confirmed that  
10 the data is recorded by high-speed transfer to a given  
address from a given address of the IC memory 4, thus  
producing a satisfactory result.

Fig. 6 is a diagram showing a fifth embodi-  
ment, in which a collective erasure function circuit is  
15 added to the circuit of Fig. 4 showing the fourth  
embodiment. The present embodiment, taking note of the  
fact that the above-mentioned digital memory is capable  
of high-speed operation, has been conceived for produc-  
ing a greater convenience. This embodiment also  
20 includes an alarm function for securing safety of the  
operation. One of various specific examples will be  
described. Specifically, this embodiment has added  
thereto an AND gate circuit 51 inserted between the  
serial-parallel conversion shift register 44 and the  
25 data selector 46, an OR gate circuit 52 inserted in the  
output of an 1/n counter 45, a collective erasure  
execution switch 53, monostable multivibrators 54 for  
generating a pulse of about a second, an OR gate circuit

1 56 for producing a logic sum of the outputs of the two  
multivibrators, a variable-frequency (about 800 Hz and  
one kHz) pulse generator 57, an AND gate circuit 58 for  
gating the output of the pulse generator, an analog  
5 signal adder circuit 59 inserted in the output side of  
the output amplifier 7 (See Fig. 1), a flip-flop 60 for  
the collective erasure execution flag, a pulse generator  
61 for generating an erasure pulse and an AND gate  
circuit 62 for gating the output of the pulse generator  
10 61. First, by turning the mode switch 47 to the EXT/  
ERASE side, the data selector 46 enters an external mode  
and stands by. When the collective erasure (for clearing  
all the contents of the IC memory 4) execution  
switch 53 is depressed in this state, the first mono-  
15 stable multivibrator 54 is energized, so that the gate  
circuit 58 is kept open for about a second, thereby  
passing the pulse signal of about 800 Hz produced from  
the pulse generator 57, so that the earphone (or the  
speaker) is started with a vibration sound of 800 Hz  
20 through the analog signal adder circuit 59. Upon the  
lapse of about a second, the second monostable multi-  
vibrator 55 is energized, followed by the generation of  
a pulse of one second. Since the transmission frequency  
of the pulse generator 57 is thus modulated to about one  
25 kHz, the output from the earphone changes to the vibra-  
tion sound of one kHz. By detouching the execution  
switch 53 under depression at a timing when the one kHz  
cheeping sound is audible, the flip-flop 69 is set,

1 thereby executing the collective erasure operation.  
Specifically, the pulse signal of 800 kHz produced from  
the pulse generator 61 is passed through the AND gate  
circuit 62, and through the OR gate circuit 52 and the  
5 data selector 46, forms a write signal (WE) of the IC  
memory 4. In the process, the write data is all zero  
(low level) since the AND gate circuit 51 is inhibited.  
Such an erasure operation as this is started from the  
zero address of the address counter (the address counter  
10 24 in Fig. 3, for instance), and is ended with the  
completion of erasure of the IC memory 3 (usually, upon  
detection of an overflow of the address counter).

According to the fifth embodiment under  
consideration, all the data recorded (a data of one  
15 volume of tape in the case of the cassette tape  
recorder) can be erased instantaneously (in about three  
seconds for a five-minute data according to the present  
embodiment), and in order to prevent an erroneous  
erasure by operation error, the operator's attention may  
20 be called merely by adding a simple circuit, thus making  
it possible to provide a system superior in operability.  
By the way, it is also possible to add a circuit for  
calling the operator's attention visually by the use of  
liquid crystal display or the like. Also, by providing  
25 a flag switch indicating a ROM mode (equivalent to a  
pawl for prohibition of recording in the cassette tape)  
and by confirming the state of the switch at the time of

1 executing erasure (or recording) at the same time, a  
system very convenient to operate is provided.

Fig. 7 shows a circuit according to a sixth  
embodiment. A large-capacity capacitor (0.1 F according  
5 to this embodiment) 72 is always kept charged through a  
resistor 71 from the positive electrode side of a  
button-type lithium battery 13. On the other hand, the  
ends of this large-capacity capacitor 72 are connected  
to the circuit section of the embodiment in Fig. 1 to  
10 supply (discharge) circuit power.

According to this embodiment, the source  
voltage does not decrease very much even when an IC  
memory is operated at high speed such as for high-speed  
dubbing (high-speed data transfer) or collective  
15 erasure, thus leading to the effect of preventing a  
false circuit operation.

When a memory is subjected to high-speed  
read/write operation, the circuit current increases  
greatly. According to this embodiment (800 kHz, 1.2  $\mu$ s  
20 cycles), the current which should be 6 to 8 mA under  
normal recording or reproduction increases to 40 to 50  
mA, and the output voltage of the lithium battery 13  
drops from 6 V (two cells of 3.0 V in rated output are  
connected in series) to 4.2 V, causing a false circuit  
25 operation. This is because a button-type lithium  
battery has such a characteristic that its output  
voltage sharply drops when the discharge current thereof  
is large, if for only a short time. Since a large-

1 capacity capacitor is always kept charged even during  
standby state and also has a large charge capacity,  
however, a short-time pulse-like discharge does not  
substantially decrease the terminal voltage, thereby  
5 assuring the normal operation of the circuit.

Fig. 8 shows a circuit according to a seventh  
embodiment. This diagram shows a case in which a DA  
converter is substituted for the AD converter shown in  
Fig. 1 according to the first embodiment and one DA con-  
10 verter is shared by the embodiments. The operation of  
the AD converter will be explained. First, a multiplex-  
er (which may alternatively be a switch) 85 is set to  
fall to the recording side. A signal that has passed  
through a low-pass filter 2 is applied to one of the in-  
15 puts of an analog comparator 80. In the process, when a  
flip-flop 81 is set by the sampling clock of a control  
circuit 8, an AND gate 82 opens, and pulses from a pulse  
oscillator 83 are supplied to a counter 84 to start  
counting. The output of the counter 84 is outputted to  
20 the DA converter 5 through the multiplexer 85, and the  
output of the DA converter 5 is outputted to the other  
input of the analog comparator 80. Therefore, the con-  
tents of the counter 84 are immediately converted into  
an analog amount and are compared with an input signal.  
25 Since the counter 84 is reset by the sampling clock, the  
output signal of the DA converter initially stands at 0  
volt. Each time a pulse is outputted to the counter 84,  
however, the analog amount sequentially increases, and



1 when it finally increases beyond the input signal, a  
signal from the comparator 80 is outputted, thereby  
immediately resetting the flip-flop 81. As a result,  
the AND gate is closed so that the counter 84 holds its  
5 prevailing state. In other words, the audio input  
information has been converted into a digital amount.  
Also, the output signal from the analog comparator 80 is  
one indicating the end of AD conversion. The control  
circuit 8 that has received this signal generates a  
10 write strobe signal for the IC memory, and writes a  
digital data into the IC memory 4. Subsequently,  
similar operations are repeated while accumulating input  
information in exactly the same manner as in the first  
embodiment. At the time of reproduction, on the other  
15 hand, the multiplexer 85 falls to reproduction side by a  
command from the control circuit 8, and the output of  
the IC memory is connected to the input of the DA  
converter 5. This operation is the same as in the first  
embodiment, and therefore will not be explained.

20 According to the present embodiment, a DA  
converter doubles as an AD converter, and therefore the  
chip area is reduced greatly, resulting in a great  
improvement of yield. Further, even when this circuit  
configuration is applied to individual parts or in the  
25 form of hybrid IC, the most expensive AD converter is  
eliminated. The system is thus reduced not only in size  
but in cost. By the way, there are of course many other  
methods of substituting one circuit for another.

1            Fig. 9 shows a circuit according to an eighth  
embodiment. The object of this circuit is to divide an  
IC memory into given sizes (blocks) for recording and  
also to make possible selective reproduction, i.e.,  
5    search, by designating the desired block with an  
operating button or the like in advance at the time of  
reproduction, in the case where there are a plurality of  
contents to be recorded. Basically, this embodiment is  
the same as the first embodiment shown in Fig. 1,  
10    although the present embodiment is configured of a block  
memory 91 for setting an address counter 24 for deter-  
mining a recording/reproduction address of an IC memory,  
a block memory address counter 97 for designating an  
address of the block memory 91, a decoder circuit 98 for  
15    decoding the contents of the block memory address  
counter, a display unit 99 for displaying the contents  
decoded, a block switch 94 for selecting a block, and a  
chatter killer circuit 95 for removing chatters. This  
circuit section is supplied with a PLAY signal (a pulse  
20    having a width of 100 ns) outputted at the time of  
depressing a PLAY switch, a RECSTOP signal (a pulse  
having a width of 100 ns) outputted at the press of a  
STOP switch at the time of recording operation. Next,  
the operation of this circuit will be explained. To  
25    facilitate understanding, assume that the block memory  
address counter 97 is at zero, and the address counter  
24 is also zero. Under this condition, when the  
recording mode is entered, a data is sequentially

1 recorded from the 0 address of the IC memory 4. Now,  
when the STOP switch is depressed in a given timing, the  
block memory address counter 97 is incremented by +1 at  
the leading edge of the RECSTOP signal (the contents  
5 therefore become 1). Further, the contents of the  
address counter 24 are memorized (making up a head  
address of the second data) at the address 1 of the  
block memory 91 through a delay circuit 92 f 100 ns.  
Next, while depressing the REC switch for recording  
10 another data, the PLAY switch is depressed. Then, the  
contents at address 1 of the block memory 91 recorded  
previously are loaded (set) in the address counter 24  
directly as a head address, and the second data are  
sequentially recorded. In similar fashion, each time  
15 the STOP switch is depressed subsequently, the contents  
of the address counter 24 are written into the block  
memory 91. The processes for reproduction, on the other  
hand, are as explained below. First, when it is desired  
to reproduce an intended data, say, a second data, the  
20 block memory address counter 97 is incremented each time  
the BLOCK switch 94 is depressed, and the contents  
thereof are displayed on a numerical display unit (which  
may be a LED display) through a decoder circuit 98. The  
BLOCK switch 94 is kept depressed until the intended  
25 address 1 (the second head address is stored in address  
1) is displayed, and when address 1 appears, the depres-  
sion is released. Next, when the PLAY switch is  
depressed, a PLAY signal is outputted, and the contents

1 of the address 1, that is, the head address recorded  
with the second data is loaded (set) in the address  
counter 24, thereby proceeding with the reading. By the  
way, when it is desired to reproduce the first data  
5 (this is also the case with recording), the incrementing  
operation of the block memory address counter 97 is  
centered at the time point of display of zero on the  
display unit 99, whereby the all-zero output of the  
decoder 98 falls to low level, so that the PLAY signal  
10 passes through the gate circuit 90 and clears the  
address counter 24. As a result, the IC memory 4  
performs the reproducing (or recording) operation from  
address zero, thus reproducing (or recording) the first  
data.

15 As explained above, according to the present  
embodiment, an intended block can be selected as desired  
by a simple operation, thus providing a system very  
convenient to handle. Another feature of the present  
embodiment is that the block length is determinable  
20 quite as desired, and the IC memory can be used with  
high efficiency without any waste. This represents a  
case in which the performance of a memory is fully  
utilized indicating the effectiveness of the system  
proposed herein.

25 Next, several embodiments relating to specific  
constructions of the present invention will be  
explained.

1            Fig. 10 shows a ninth embodiment. In the  
drawing, 101 designates a body for sound recording and  
reproduction section including an A/D (analog/digital)  
converter for converting an analog signal into a digital  
5    signal, a D/A (digital/analog) converter for converting  
a digital signal into an analog signal and a control  
circuit. 103 designates a memory card for storing a  
voice, and 102 an I/O slot making up a socket for the  
memory card 103 connected at a connecting terminal in  
10   the body 101. Further, 104 designates a memory recogni-  
tion section for recognizing the type of semiconductor  
memory used by the memory card 103, such as EPROM,  
EEPROM, SRAM or DRAM. The body 101 covers the greater  
part of the memory card 103 and has a part thereof so  
15   extended outside or such a mechanical construction as to  
permit mounting and demounting of the component 103.

          The memory recognition section 104 built in as  
above is for recognizing each memory and generates an  
access signal of various memories. As a result, various  
20   types of memory cards 103 can be recorded and reproduced  
with a single body 101. Also, since the greater part of  
the housing of the memory card 103 is covered, the  
protection of the housing of the memory card 103 is  
easy, leading to the advantage that somewhat rough  
25   handling is resisted. By the way, the body 101 may be  
constructed of a transparent plastics or the like  
converted directly above the title, name or the like of

1 the memory card 103 thereby to enable the user to easily  
recognize the memory card 103 in use.

A tenth embodiment is shown in Fig. 11. In  
the drawing, the same reference numerals as those in  
5 Fig. 10 will not be described. 105, 105' designate a  
mechanism for fixing the body 101 making up a sound  
recording and reproduction section and the memory card  
103'. This embodiment is different from that of Fig. 10  
in that this embodiment has a simplified fixing  
10 mechanism and therefore can be thinned to substantially  
the same degree as the memory card 103. As a result,  
the embodiment under consideration can be reduced in  
size to a degree more than the ninth embodiment. It is  
therefore easy to carry and in addition, the simple  
15 fixing mechanism with roughness reduces the system cost.

An eleventh embodiment is shown in Fig. 12.  
In the drawing, the same reference numerals as those in  
Fig. 10 will not be described. 106 designates a trans-  
parent cover for protecting the memory card 103.

20 According to this drawing, the protection of  
the memory card 103 is easy as in the case of Fig. 10.  
Further, the name or like of the memory card 103 can be  
easily recognized due to the transparent cover 106.'

According to the above-mentioned embodiments,  
25 most of the functions of the body 101 are formed in a  
single chip, for example. By doing so, a vacant space  
can be produced in the body, and a large-capacity  
battery can be mounted. As a result, the supply of

1 large power at the time of recording or reproduction or  
the long-time operation of the memory cards 103, 103'  
inserted can be backed up.

A twelfth embodiment is shown in Fig. 13. In  
5 the drawing, 4a designates a memory for audio storage,  
8a a sound recording control circuit, and 107 an audio  
recording section configured of an amplifier 1, a low-  
pass filter 2, an A/D converter 3 and a control circuit  
8a. The audio recording section 107 has the component  
10 circuits thereof activated by a sound recording control  
signal from an external source, and the audio input  
signal is written into the audio storage memory 4a.  
Also, 4c designates an audio data signal, 8c a transfer  
control signal and 13a a power circuit of the sound  
15 recording section 107.

On the other hand, 4b designates a memory for  
storing a reproduction sound, 8b a reproduction control  
circuit, and 108 a voice reproduction section configured  
of the memory 4b, a D/A converter 5, a low-pass filter  
20 6, an amplifier 7 and the reproduction control circuit  
8b. Further, 8c designates a voice data change-over  
switch. In the case of sound recording, the voice data  
is transferred from the voice recording section 107 to  
the voice reproduction section 108 upon the instruction  
25 of the production control signal. In the case of  
reproduction, on the other hand, the reproduction  
control circuit 8b is controlled in such a manner as to  
output a voice through the D/A converter 5 from the

1 reproduction sound storage memory 4b. Further, 109  
designates an I/O slot making up a receptacle for the  
reproduction section 108 for connecting the reproduction  
section 108 at a connecting terminal in the sound  
5 recording section 107. 13b designates a power circuit  
for the reproduction section and is configured of a  
primary or secondary battery. The secondary battery has  
a charging circuit. It also has a residual amount  
10 detector circuit for displaying the residual amount of  
the battery charge to hold the data of the reproduction  
sound storage memory 4b.

The circuit shown in this drawing is such that  
the voice recording section 107 and the voice reproduc-  
tion section 108 are separated from each other, and  
15 therefore the sound recording function of 108 is not  
required, thus realizing a power-saving, compact and  
low-cost system. Also, in the case of portable type,  
the reproduction section 108 is often carried while the  
sound recording section 107 is used in fixed position in  
20 many cases. Therefore, the power circuit 13a of the  
voice recording section 107 can be supplied directly  
from an AC power supply or the like. As a result in the  
case of transferring a digital voice at high speed for  
recording or the like, the power supply for the voice  
25 reproduction section 108 easily supplies large power  
required for energizing at high speed the internal  
circuits, or the memory 4b in particular.



1           By the way, the power circuit 13a is also  
capable of backing up the storage information in the  
case where the memory 4a is of volatile type. Also, the  
circuit blocks are accommodated in the housing of the  
5 voice reproduction section 108 and the voice recording  
section 107 respectively. Further, it is of course  
possible to use similarly the functions shown in Fig. 11  
or 12, the function of recognition of the voice repro-  
duction section 108 of 104 in the voice recording  
10 section 107 and the like.

A thirteenth embodiment is shown in Fig. 14.  
In the drawing, 4 designates a memory section for  
storing a voice, 3 an A/D converter for converting an  
analog into a digital signal, 5 a D/A converter for  
15 restoring an analog signal from a digital signal, 24 an  
address counter for generating a memory address, 115 a  
control section for setting an address start position or  
the like of the memory, and 116 an AND gate for applying  
a clock to a counter. Also, 117 designates a switch SW1  
20 for switching the sampling frequency for the A/D  
converter 3, 118 a switch SW2 for switching the sampling  
frequency for the D/A converter 5, and 119, 120, 121  
circuits for generating different sampling frequencies  
 $f_1$ ,  $f_2$ ,  $f_3$ . 122 designates a voice input terminal, 123  
25 a voice output terminal, 124 a system drive terminal for  
activating the system, and 125 a read/write terminal of  
the memory for recording/reproduction. Further, 126

1 designates the whole of a recording-reproduction section including the memory section 4.

In the drawing, assume that the sampling frequencies hold the relation  $f_1 < f_2 < f_3$  and the A/D  
5 converter 4 and the D/A converter 5 are controlled independently of each other. This control is effected manually by use of an external switch. A method of this operation consists in, first, changing the switches SW1 and SW2 at the same time as a mechanism. Specifically,  
10 the recording and reproduction frequencies are made to coincide with each other. In the case where it is desired to differentiate between recording and reproduction, on the other hand, they are switched separately from each other. This may be used, for  
15 example, to search for the reproduction sound of the switches SW1, SW2 at high speed or for the like purpose. By the way, electrically, a single switch may be easily used to function for both recording and reproduction at the same time. Further, generally, in view of the fact  
20 that one of the A/D converter and the D/A converter is energized while the other is inactivated, the object of switching can be achieved with a single switch. Only the switch SW1 may be used as a change-over switch for the sampling frequencies  $f_1, f_2, f_3$ , with the terminal A  
25 of the switch SW1 connected to the D/A converter 3 and the A/D converter 5.

In the above-described embodiment, in terms of sound quality level,  $f_1$  is used for conversation,  $f_3$  for

1 music of high sound quality, and  $f_2$  for recording/repro-  
duction for applications intermediate therebetween. As  
a result, the sound quality level and the volume of the  
memory are optimized. Further, a comparatively high-  
5 speed sound recording or reproduction can be effected at  
least to a maximum speed of the D/A converter 3 or the  
A/D converter 5 against the cycle time of the memory.  
The added function of high-speed recording and  
reproduction is realized by providing a terminal for  
10 selecting a fourth sampling frequency  $f_4$  ( $< f_3$ ) in the  
switches SW1, SW2.

In the foregoing, the sampling frequency  $f_1$   
for conversation has the advantage of extending the  
battery life due to a slow recording and reproduction,  
15 and therefore the system is operable for long time  
before each change or charging of the battery. In the  
case where a music is recorded or reproduced at high  
speed for realizing a high sound quality, on the other  
hand, the sampling frequency  $f_3$  is higher in speed by  
20 about one digit than the sampling frequency  $f_1$  for  
conversation, and therefore the battery life is  
shortened. The latter frequency, however, is for  
enjoying music, and if one thinks that he or she does  
not want to hear the same music for long time, the high-  
25 speed recording function may be used on audio equipment  
by recording for a short length of time on any desired  
day. Further, for this semi-permanent storage of the  
audio information, the disadvantage involved may be

1 compensated for by transferring the information to a  
magnetic or optical disk or the like, considering the  
fact that the memory card of SRAM of battery back-up  
type now in use has a period of information storage as  
5 short as only two or three years.

Fig. 15 shows a specific arrangement of  
sampling frequency change-over switches included in the  
embodiment of Fig. 14. In the drawing, 126 designates  
the whole view of the recording-reproduction section,  
10 and 127 an operating panel section thereof, representing  
a case in which the sampling frequencies of the D/A  
converter 3 and the A/D converter 5 are switched with a  
single switch SW1. In this way, by switching the sampl-  
ing frequencies  $f_1$ ,  $f_2$ ,  $f_3$  arbitrarily, the recording  
15 and reproduction intended for efficient use of the  
memory is realized.

By the way, in another form of the present  
invention, automatic switching of sampling frequencies  
is conceivable by detecting the sound quality. The  
20 manual switching operation according to the present  
invention provides simple and effective means meeting  
the demand for recording or reproducing only the words  
of a music or the demand for recording the features of a  
human voice in a conversation or an environmental sound.  
25 The automated switching of sampling frequencies may be  
used easily in parallel to manual operation. By doing  
so, too, the object of using an efficient memory  
according to the present invention is achieved. In

1 addition, various modifications are possible without  
departing from the spirit of the invention.

Next, before a fourteenth embodiment, explanation will be made about a substrate structure, a circuit  
5 arrangement on a chip and a method of supplying a source  
voltage in the case where an AD converter, a DA converter, a control circuit and a memory are constructed  
in the same chip. In a circuit such as an AD converter  
or DA converter which handles an analog signal, it is  
10 necessary to suppress the variations in the source  
voltage, earth voltage and substrate voltage as far as  
possible from the viewpoint of S/N. In such circuits as  
a control circuit or a memory, a large load capacitor is  
driven or a through current flows to the earth voltage  
15 from a source voltage during circuit operation, with the  
result that the source voltage, the earth voltage and  
the substrate voltage undergo a great variation.  
Especially, in the case of using a one-transistor one-  
capacitor memory cell capable of being high integration  
20 as a memory, a multiplicity of data lines are charged or  
discharged simultaneously during memory operation,  
thereby causing a great variation in source voltage and  
earth voltage. Also, the substrate voltage may change  
by the capacitance coupling between a data line and the  
25 substrate. It is therefore necessary to prevent the  
variation in source voltage, earth voltage or substrate  
voltage generated in such circuits as a control circuit

1 or a memory from being transmitted to the circuits  
handling an analog signal.

In a memory such as a none-transistor one-  
capacitor memory which stores memory information in the  
5 form of presence or absence of charges, it is necessary  
to prevent the breakdown of minority carriers (electrons  
in the case of p-type silicon substrate) injected into  
the substrate. These minority carriers are injected  
into the substrate when an external noise (generally, a  
10 surge noise such as undershoot) is inputted to the  
input-output terminals of the chip. This may also be  
caused in the operation of a control circuit, when the  
potential of the substrate or the diffusion layer  
locally undergoes a change by the capacitance coupling.  
15 As a result, it is necessary to prevent the minority  
carriers generated in the circuits other than the memory  
or the input-output terminals from being transmitted to  
the memory section.

The two problems were described above which  
20 are caused when an AD converter, a DA converter, a  
control circuit and a memory configure a single chip.  
An example of the substrate structure of the chip for  
solving them will be explained with reference to the  
fourteenth embodiment shown in Figs. 16 and 17. Fig. 16  
25 shows a case intended to solve the problems by  
electrically isolating the substrate regions forming a  
MOS transistor by a double-formed well layer. Fig. 16  
shows a n-channel MOS transistor (NMOS) and a p-channel

1 transistor (PMOS), one each for the control circuit  
section and a circuit handling an analog signal (analog  
section). Characters S, G and D of the NMOS and PMOS  
designate terminals of the source, gate and the drain  
5 respectively. Also, this embodiment represents a case  
in which the one-transistor one-capacitor memory cell is  
used as a memory cell. The memory cell forms an  
accumulated capacity between the n-type diffusion layer  
(the impurities diffusion layer is described only with  
10 conduction type of impurities for simplicity sake in the  
drawing) and the plate (PL). Charges are accumulated in  
this accumulation capacitor. This memory information is  
read onto or written from a data line (DL) by control-  
ling a gate connected to a word line (WL).

15 Now, as shown in the drawing, an n-type well  
layer NW1 is formed in a p-type substrate (p-sub), and  
further a p-type well layer pw1 therein. And a memory  
cell is formed in this p-type well layer pw1. The MOS  
transistor in the control circuit section, on the other  
20 hand, has an NMOS formed in the p-type well layer pw2  
formed in the p-bus, and a PMOS in the n-type well layer  
nw1 formed in p-sub. Also, the analog section, like the  
memory section, has an n-type well layer NW2 formed in  
the p-type substrate (p-sub), and further a p-type well  
25 layer pw3 and an n-type well layer nw2 therein. And an  
NMOS is formed in this p-type well layer pw2 and a PMOS  
in the n-type well layer nw2.

1           In this structure, each well layer is supplied  
with voltage VB1 to VB6. In the case where the circuit  
is operated between the source voltage Vcc (say, 5 V)  
and the earth voltage (0 V), the voltages applied  
5 include, as an example:

$$VB1 = 0 \text{ V}$$

$$VB2 = 5 \text{ V}$$

$$VB3 = 0 \text{ V}$$

$$VB4 = 5 \text{ V}$$

$$VB5 = 0 \text{ V}$$

$$VB6 = 5 \text{ V}$$

Specifically, voltages are applied in such a manner that  
the junction between the p-type well layer and the n-  
type well layer and that between the diffusion layers  
(n, p) and the well layers are not biased in forward  
10 direction.

By doing so, first, the MOS transistor of the  
analog section formed in the n-type well layer NW2 is  
electrically isolated from the p-sub, and is not  
affected by the variations in the substrate voltage (or  
15 the well voltage) generated in the memory section or the  
control circuit section. Also, if the input-output  
terminals are disposed in the control circuit section,  
the minority carriers injected from the input-output  
terminals or generated in the control circuit section  
20 are absorbed into the n-type well layer NW1, thereby



1 preventing the breakage of the stored information which  
otherwise might be caused thereby. Further, since the  
well voltages of the respective circuit sections can be  
set independently of each other, it is also possible to  
5 apply a well voltage most suitable for the character-  
istic of each circuit. In the memory section, for  
instance, a negative voltage but not the earth potential  
may be applied to the p-type well layer pw1 for the  
purpose of reducing the parasitic capacitance of the  
10 data line.

By the way, although the example of Fig. 16  
shows only one MOS transistor in one well layer, a  
plurality of transistors are formed generally in the  
same well layer. Also, a plurality of well layers of  
15 the same conduction type may be formed in the n-type  
well layer NW1 or NW2. In addition, different voltages  
may be applied to these well layers to such an extent  
that the junctions are not biased in forward direction.  
As such an example, the source terminal of a MOS  
20 transistor and a well layer are desirably connected in a  
circuit handling an analog signal. This is in order to  
suppress the variations in the threshold voltage due to  
the source potential by always maintaining the source  
and well potentials at the same level.

25 Further, although the p-type well layer pw2 is  
inserted in the control circuit section in Fig. 16, the  
well layer which is of the same conduction type as the  
p-sub may be eliminated but the NMOS of the control

1 circuit section may be formed directly in the p-sub.  
This is also the case with the n-type well layer nw2 of  
the analog section.

Furthermore, unlike in the example of Fig. 16  
5 where the n-type well layer NW1 is formed in the memory  
section, the memory section and the control circuit  
section, if these alone are taken note of, are  
configured in the same way as a dynamic random access  
memory (DRAM). Therefore, the n-type well layer NW1 is  
10 not formed, but it is generally possible to solve the  
problem of minority carriers by applying a negative  
voltage (say, -3 V) to the p-sub as in the case of DRAM.  
This negative voltage may be either generated within the  
chip or applied from a source outside of the chip.

15 As described above, in order to eliminate the  
effect of minority carriers or variations in the  
substrate voltage, the substrate regions forming a MOS  
transistor of the memory, the control circuit and the  
analog section are electrically isolated by a double-  
20 formed well layer. Electrical isolation of the  
substrate regions, however, is not limited to the  
methods described herein. It is alternatively possible  
by using a substrate of the SOI (silicon on insulator)  
structure. Also, if an epitaxial substrate is used,  
25 though complete electrical isolation may be impossible,  
the effect of variations in the substrate voltage can be  
suppressed by a high-resistance epitaxial layer.

1            Now, a method of supplying a source voltage  
and a circuit arrangement within a chip will be  
explained. As described above, the variations in the  
source voltage or the earth voltage cause in the control  
5 circuit or the memory section are required to be  
prevented from being transmitted to the circuits  
handling an analog signal. For this purpose, it is  
necessary to isolate the power lines for supplying the  
source voltage or the earth voltage between the control  
10 circuit or the memory section and the circuits handling  
an analog signal. Also, if the memory operation is to  
be stabilized, it is desirable to isolate the power  
lines between the control circuit and the memory  
section. The circuit arrangement in the chip,  
15 therefore, should be such that the control circuit, the  
memory section and the circuits handling an analog  
signal are arranged in blocks respectively so that the  
source voltage and the earth voltage may be supplied  
independently to the memory, the control circuit, the AD  
20 converter and the DA converter independently of each  
other. By this arrangement in blocks, the substrate  
structure described above becomes easy to form. Also,  
as to the well voltage described with reference to Fig.  
16, the well voltage for each circuit section may be  
25 connected to the source voltage and the earth voltage  
for each circuit section, or a voltage may be supplied  
from an exclusive pin if there are a sufficient number of  
pins of the chip.

1                   Considering the scale of each circuit, on the  
other hand, the memory section occupies the largest  
proportion of the chip area of all the circuits  
including the control circuit and the circuits handling  
5 an analog signal. In the case where a voice is  
digitized at the sampling frequency of 8 kHz and 4 bits,  
for example, the 30-minute recording requires the memory  
capacity of about 60 Mbits. In comparison, the control  
circuit, the AD converter or the DA converter can be  
10 configured of several k gates in terms of the number of  
logic gates. As a result, the circuits should be  
arranged in the chip in such a manner that the control  
circuit, the AD converter and the DA converter are  
disposed in blocks along one or two sides of the memory  
15 section that occupies the greater part. A specific  
example of circuit arrangement in the chip is shown in  
Figs. 17(a) to (d).

                  Figs. 17(a) and (b) show a case in which the  
control circuit C, the AD converter A and the DA  
20 converter D are arranged along one side of the memory  
section. The control circuit C, the AD converter A and  
the DA converter D are arranged in parallel in Fig.  
17(a), and in two stages in Fig. 17(b). In these  
arrangements, an analog input signal  $A_{in}$  inputted from  
25 outside the chip is digitized by the AD converter A and  
is stored in the memory. Also, the digitized signal is  
read out of the memory, converted into an analog signal  
by the DA converter D, and is outputted outside the chip

1 as an analog output signal Aout. In this manner, by  
arranging the control circuit C, the AD converter A, the  
DA converter D and the memory section in blocks on the  
chip collectively, the power lines are isolated easily  
5 as mentioned above. In addition, the substrate  
structure described with reference to Fig. 16 is easily  
formed. Fig. 17(c) shows another embodiment of circuit  
arrangement in the chip, and represents a case in which  
the memory section is divided into two blocks, between  
10 which the control circuit C, the AD converter A and the  
DA converter D are arranged. As well known, with the  
increase in memory capacity, the signal wires in the  
memory section are lengthened, sometimes posing the  
problem of signal delay due to the parasitic resistor or  
15 parasitic capacitance thereof. In such a case, the  
signal delay can be reduced by dividing the memory  
section and shortening the length of the signal wires.  
Such an example is shown in Fig. 17(c), in which the  
memory section is divided into two parts, between which  
20 the control circuit C, etc. are arranged with the  
intention of reducing the signal delay of the memory  
section. Fig. 17(d) shows a case in which the memory  
section is divided into four blocks, between which the  
control circuit C, the AD converter A and the DA  
25 converter D are arranged, whereby the signal delay of  
the memory section is further reduced.

In the case where a memory of dynamic type  
such as a one-transistor one-capacitor memory is used

1 as a memory, as well known, it is necessary to perform  
the refreshing operation for refreshing the storage  
information at predetermined time intervals in order to  
hold the storage information. Unless this refreshing  
5 operation is performed, however, the storage information  
accumulated in the memory would be lost, thereby making  
it possible to form a fixed pattern of information in  
the memory. In other words, the information in the  
memory could be erased collectively. A fifteenth  
10 embodiment for realizing this is shown in Fig. 18. In  
Fig. 18, the operation of a memory of dynamic type is  
controlled by a control signal MS, and when this signal  
is at low potential, the memory performs the reading,  
writing and refreshing operations. A signal such as RAS  
15 is used as this signal in DRAM, for example. Under  
normal operation, this signal is generated through a  
NAND circuit by the control signal MS generated from a  
control circuit. The signal RS is for controlling the  
collective erasure of the memory and maintains a high  
20 potential under normal operation while assuming a low  
potential for a certain length of time when the  
collective erasure is designated. This signal is  
generated when a switch for collective erasure provided  
in the system is turned on, and by using an oscillator  
25 provided in the system, the time for which its low  
potential is maintained can be controlled. In such a  
configuration as this, the signal RS is at high  
potential under normal operation, and the memory

1 operation can be controlled by the control signal MS  
generated from the control circuit. In the case where  
collective erasure is designated, on the other hand, the  
signal RS maintains a low potential for a certain length  
5 of time, and the memory remains unenergized as the  
control signal MS becomes high in potential during the  
same period. Specifically, during such a period, no  
refreshing operation is performed. After that, when the  
signal RS becomes high in potential, the normal opera-  
10 tion is restored. The time during which the signal RS  
is maintained at low potential is the one during which  
all the information in the memory is lost for lack of  
the refreshing operation, and may normally be several  
hundred seconds.

15           The collective erasure by this method is  
effected by suspending the operation of the memory, and  
therefore the power consumption of the memory can be  
reduced. Conventionally, it was necessary to write  
fixed information (information "0" or "1") in a memory  
20 cell in order to erase the information in the memory.  
As compared with such a conventional method, the present  
embodiment can minimize power consumption. As a result,  
the life of the battery in the system can be lengthened.

          Also, according to this method, the time  
25 required for collective erasure of the memory is not  
dependent on the memory capacity. Even when a large-  
capacity memory is provided in the system, therefore,

1 the great advantage is that the time required for  
collective erasure is not increased.

[Effect of the Invention]

5 According to the present invention, a reliable  
system small in size and power consumption is provided  
for recording and reproducing analog information such as  
a voice without using any mechanical parts such as a  
motor.

#### 4. Brief Description of Drawings

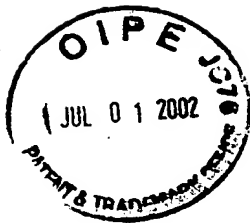
10 Fig. 1 is a functional block diagram showing a  
first embodiment, Fig. 2 is a block diagram showing a  
second embodiment, Fig. 3 is a block diagram showing a  
third embodiment, Fig. 4 is block diagram showing a  
receiving section of a fourth embodiment, Fig. 5 is a  
15 block diagram showing a transmitting section of the  
fourth embodiment, Fig. 6 is a block diagram showing a  
fifth embodiment, Fig. 7 is a circuit diagram showing a  
sixth embodiment, Fig. 8 is a circuit diagram showing a  
seventh embodiment, Fig. 9 is a circuit diagram showing  
20 an eighth embodiment, Fig. 10 is a structural diagram  
showing a ninth embodiment, Fig. 11 is a structural  
diagram showing a tenth embodiment, Fig. 12 is a  
structural diagram showing an eleventh embodiment, Fig.  
13 is a structural diagram showing a twelfth embodiment,  
25 Fig. 14 is a circuit diagram showing a thirteenth  
embodiment, Fig. 15 is an outside view showing the  
thirteenth embodiment, Fig. 16 is a diagram showing an



- 1 LDSUI structure according to a fourteenth embodiment, Fig. 17 is a diagram showing a circuit arrangement of LSI, and Fig. 18 is a block diagram showing a fifteenth embodiment.

1 ... Input amplifier, 2 ... Input-side low-pass filter, 3... AD converter, 4 ... Ic memory, 5 ... DA converter, 6 ... Output-side low-pass filter, 7 ... Output amplifier, 8 .. control circuit, 13 ... Button-type lithium battery, 14 ... Memory chip integrated circuit, 15 .. Base substrate, 21 .. Tri-state buffer, 23 ... Delay circuit, 24 ... Address counter, 25 ... Digital comparator, 27 ... FIFO memory, 31 ... Data selector, 32 ... Ternary counter, 35 ... Nonlinear circuit, 543 ... PLL transmitter, 44 ... Serial-parallel conversion shift register, 46 ... Data selector.

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DECLARATION

Technology Center 2100

I, Michiyuki MORITA , a national of Japan, c/o Asamura Patent Office of 331-340, New Ohtemachi Building, 2-1, Ohtemachi-2-chome, Chiyoda-ku, Tokyo, Japan do hereby solemnly and sincerely declare:-

- 1) THAT I am well acquainted with the Japanese language and English language, and
- 2) THAT the attached is a full, true and faithful translation into the English language made by me of Japanese Patent Application No. 3-57930

The undersigned declares further that all statements made herein of his own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001, of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Signed this 31st day of January , 1994.

Michiyuki Morita

Michiyuki MORITA

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[Reference Number] H1002541

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[Addressee] The Director-General  
The Patent Office

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[Title of the Invention] DATA CONVERSION SYSTEM AND  
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[Number of Claim(s) for a Patent] 5

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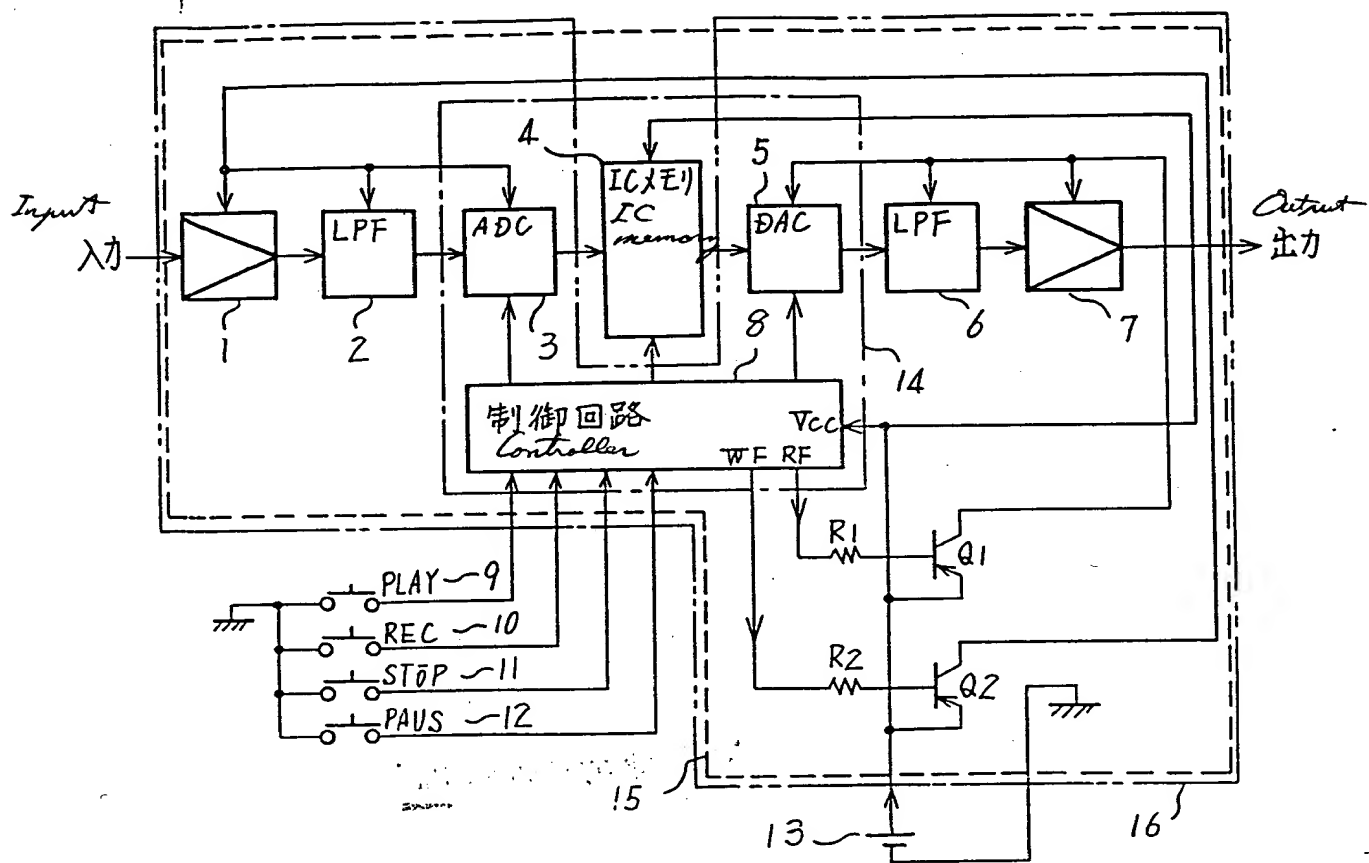
## [Indication of Fee]

[Way of Payment] Prepayment  
[Prepayment Register Number] 000376  
[Amount of Payment] ¥14,000-

## [List of Items Filed]

[Title of Article]	Specification -----	1
[Title of Article]	Drawing -----	1
[Title of Article]	Abstract -----	1
[Number of General Power]	9003106	

第 1 図 Fig. 1



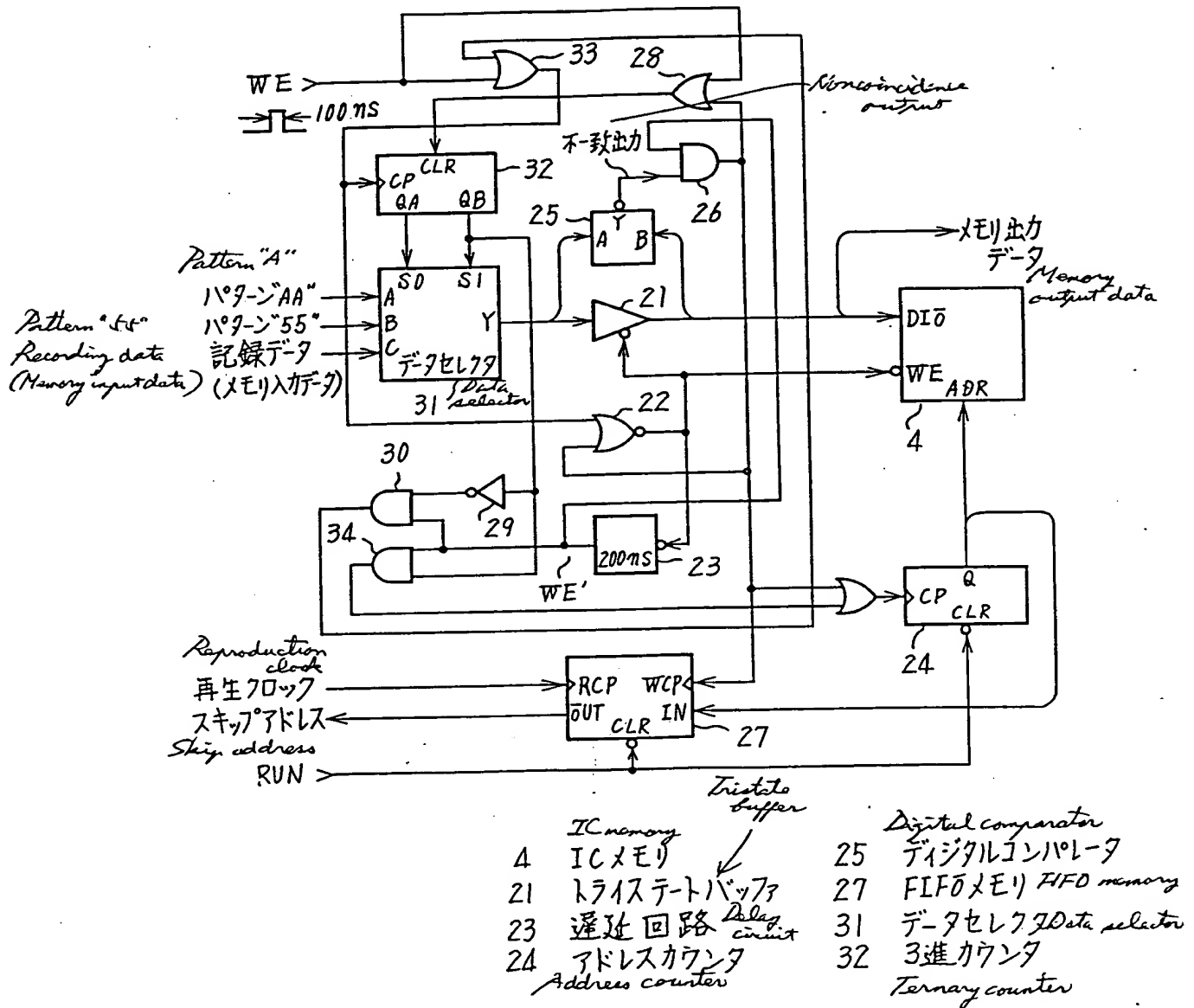
- |                             |               |                       |
|-----------------------------|---------------|-----------------------|
| Input-side low-pass filter  | 1 入力増幅器       | 7 出力増幅器               |
| AD converter                | 2 入力側低域通過フィルタ | 8 制御回路 Controller     |
| IC memory                   | 3 AD変換器       | 13 電池型リチウム電池          |
|                             | 4 ICメモリ       | 14 メモリチップ Memory chip |
| DA converter                | 5 DA変換器       | 15 ベース基板 Base board   |
| Output-side low-pass filter | 6 出力側低域通過フィルタ | 16 ハイブリッドIC Hybrid IC |

Button-type lithium battery

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代理人 小川 勝 男

第 2 図 Fig. 2

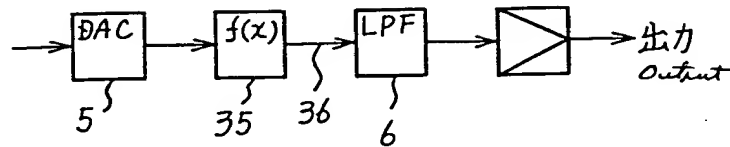


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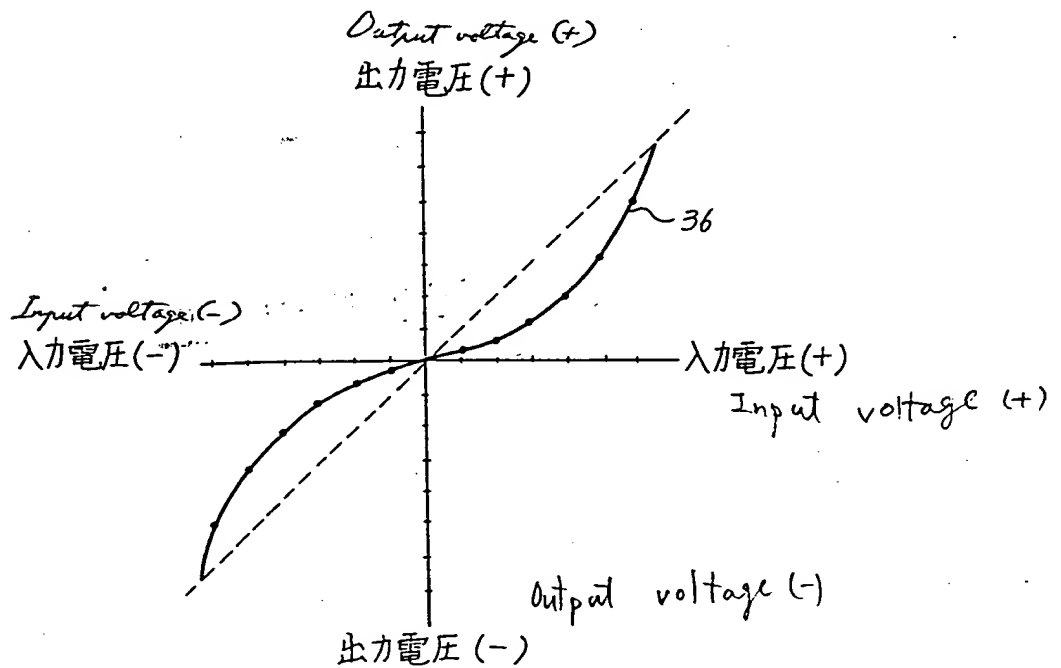
代理人 弁護士 小川 勝男

第 3 図 Fig. 3

(a)

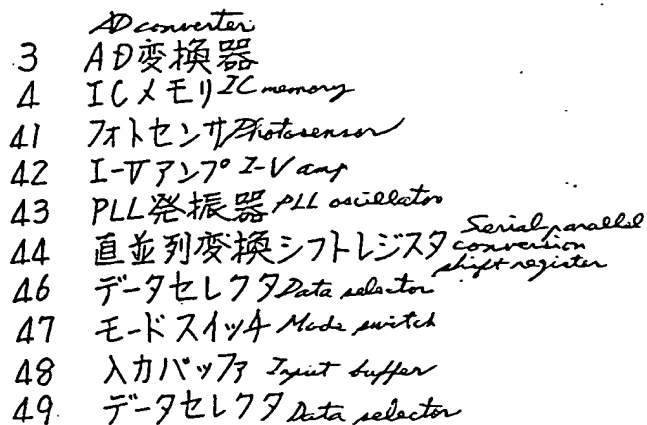


(b)



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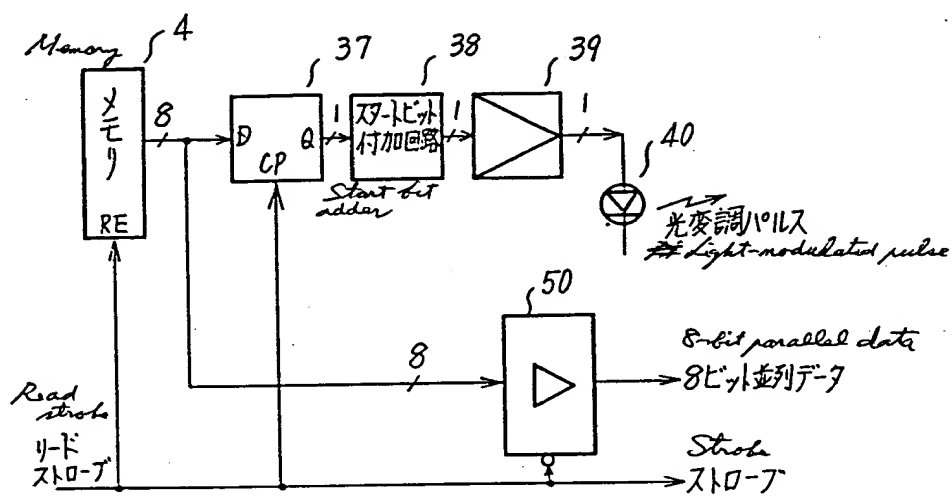
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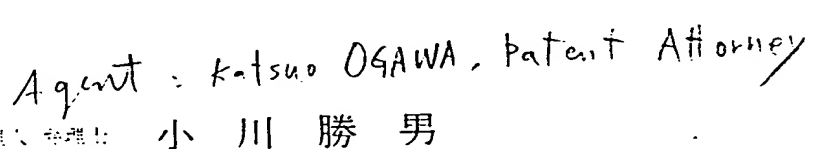
第 5 図 Fig. 5



- Serial parallel conversion shift register
- 37 直並列変換シフトレジスタ
  - 38 スタートビット付加回路 Start bit adder
  - 39 V-I アンプ V-I amp
  - 40 レーザダイオード Laser diode
  - 50 出力バッファ Output buffer
  - 4 ICメモリ IC memory

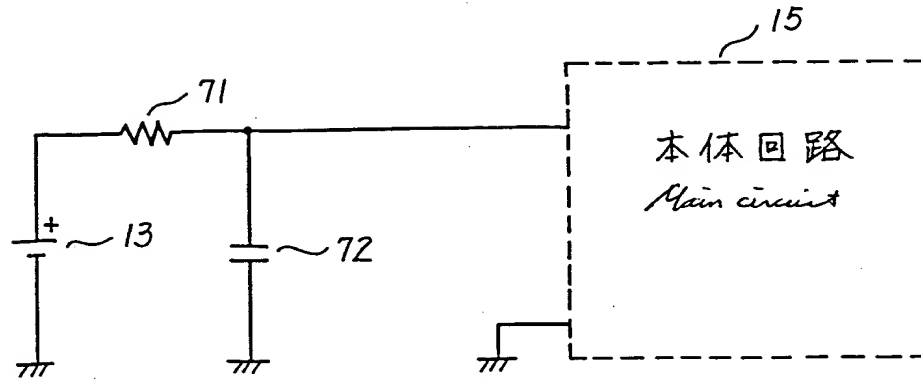
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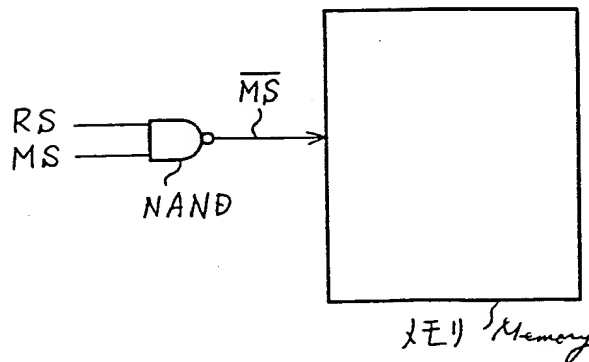
다들! 다들!

第 7 図 Fig. 7



- Button-type lithium battery cell  
 13 ボタン型リチウム電池  
 15 ベース基板 (本体) Base board (body)  
 71 抵抗 Resistor  
 72 大容量コンデンサ Large-capacity capacitor

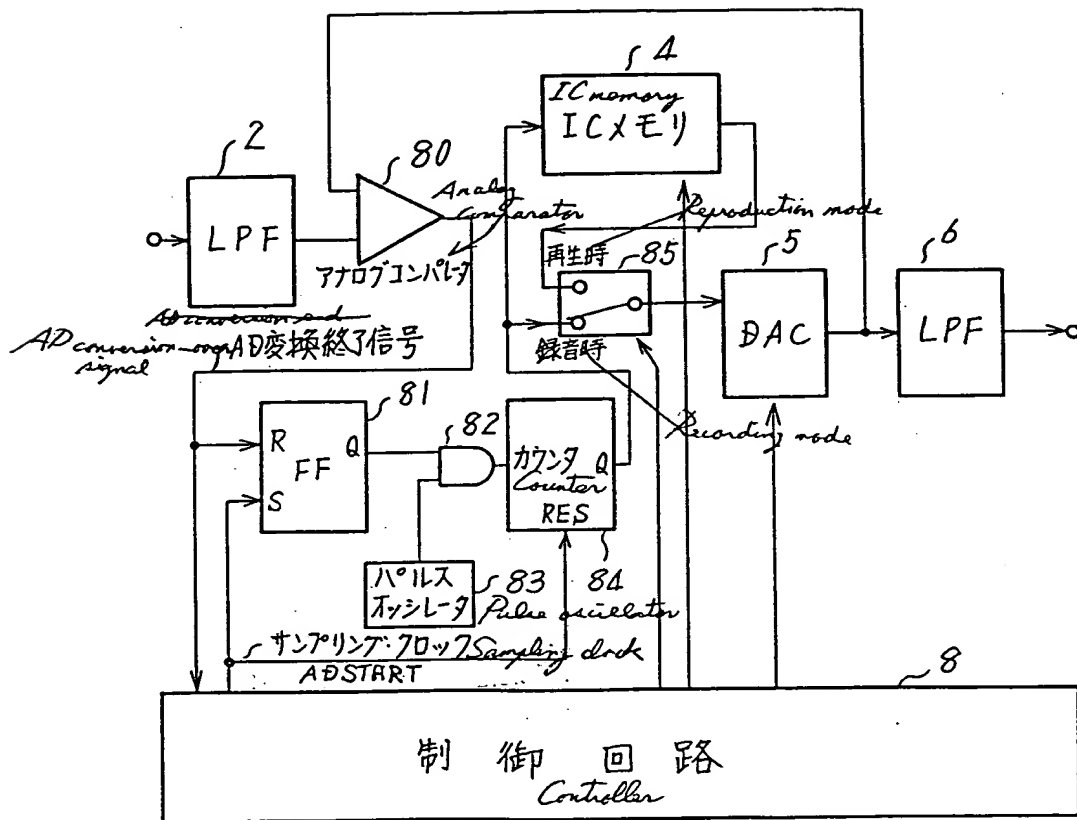
第 18 図 Fig. 18



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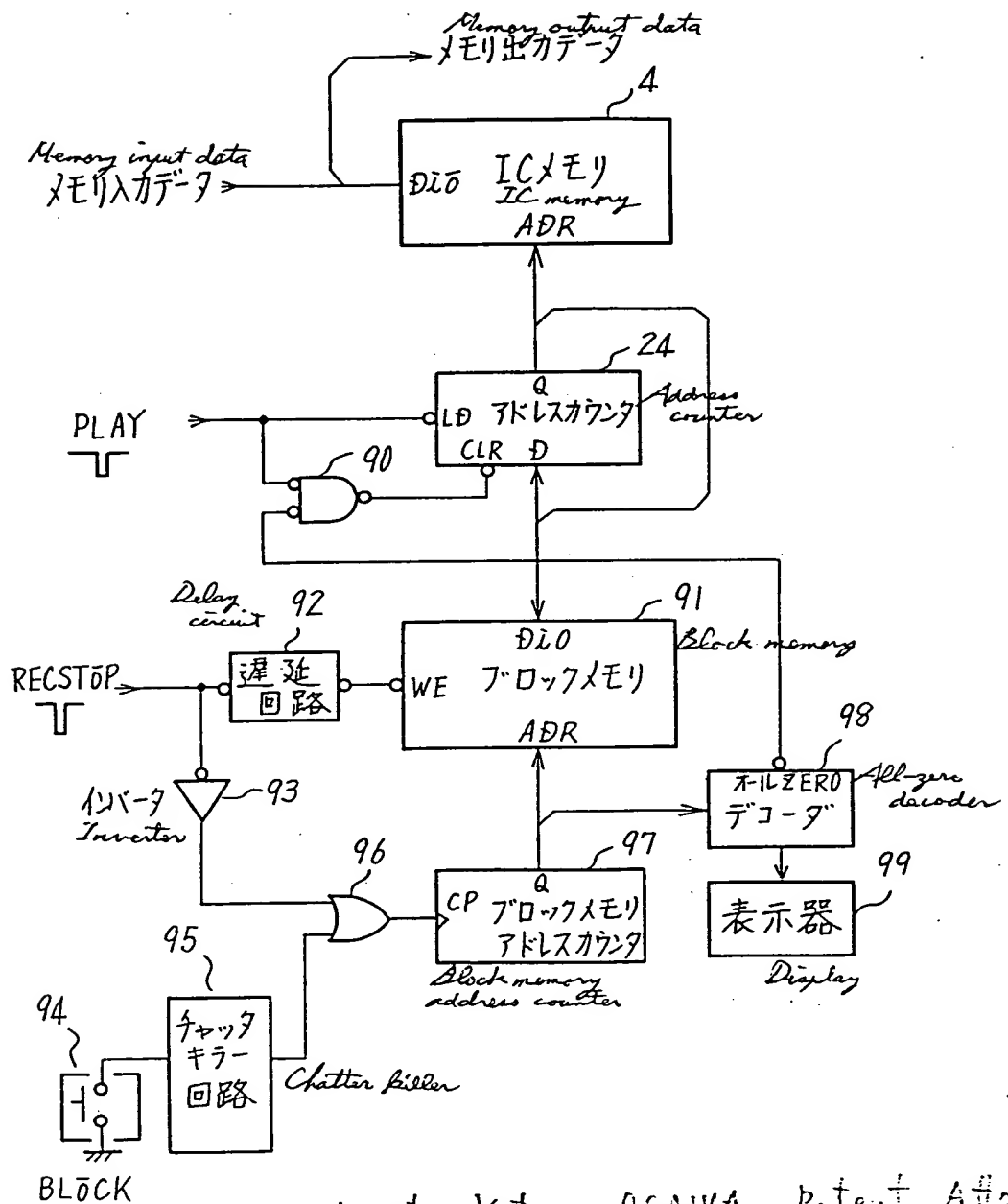
第 8 図 Fig. 8



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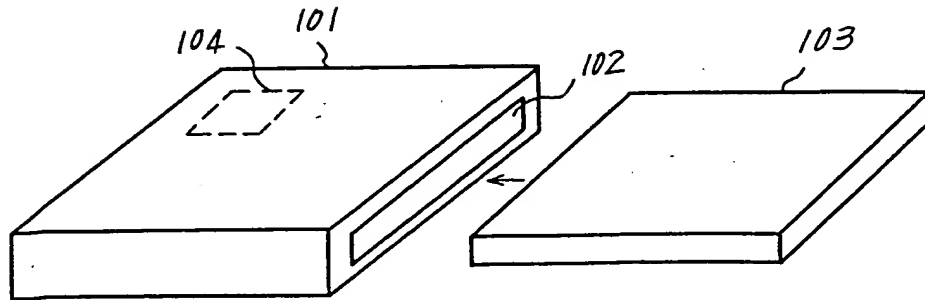
第 9 図 Fig. 9



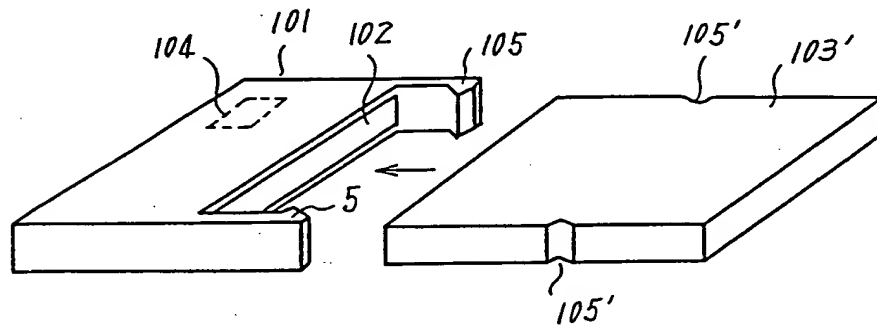
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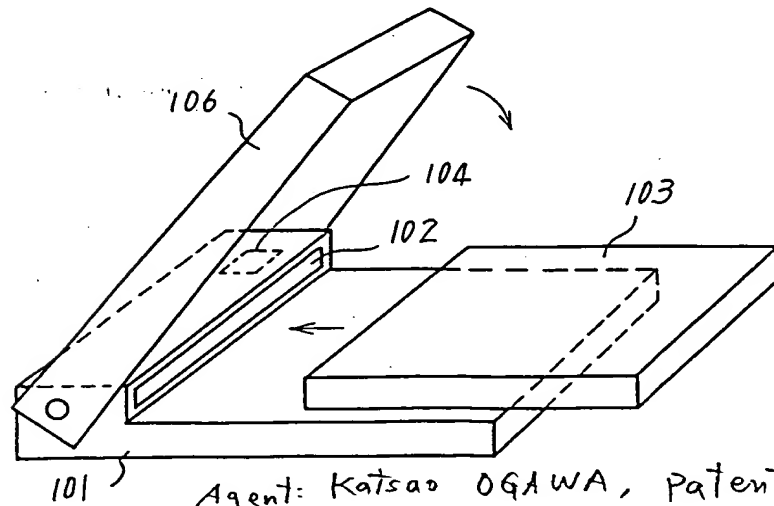
第 10 図 Fig. 10



第 11 図 Fig. 11



第 12 図 Fig. 12

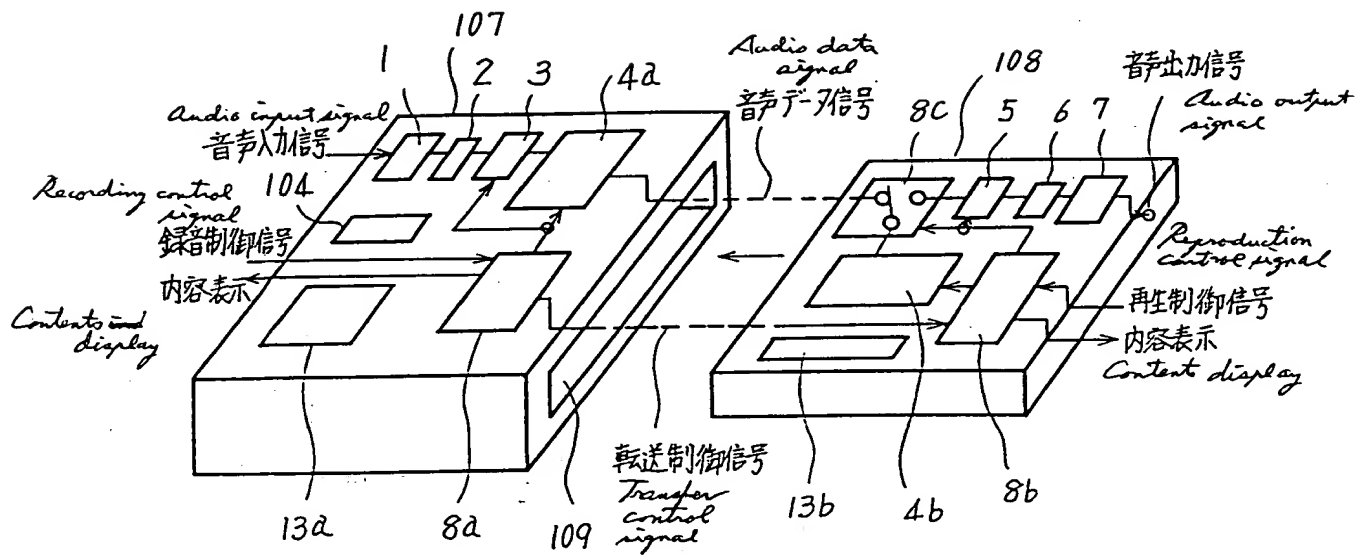


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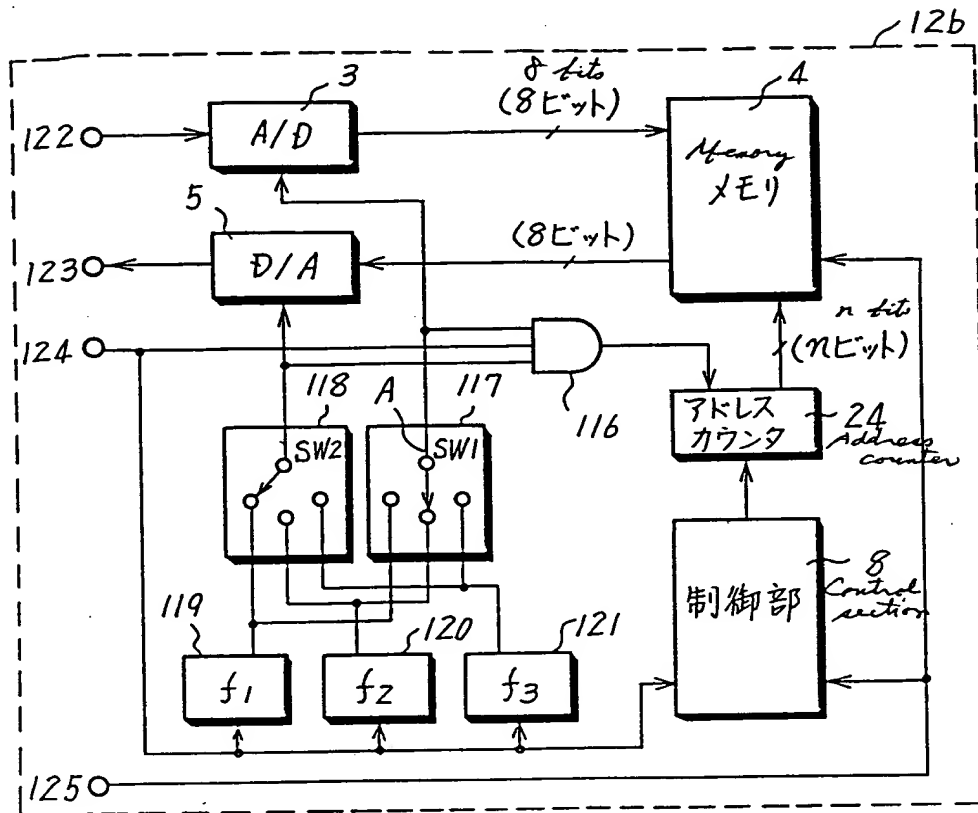
第 13 図 Fig. 13



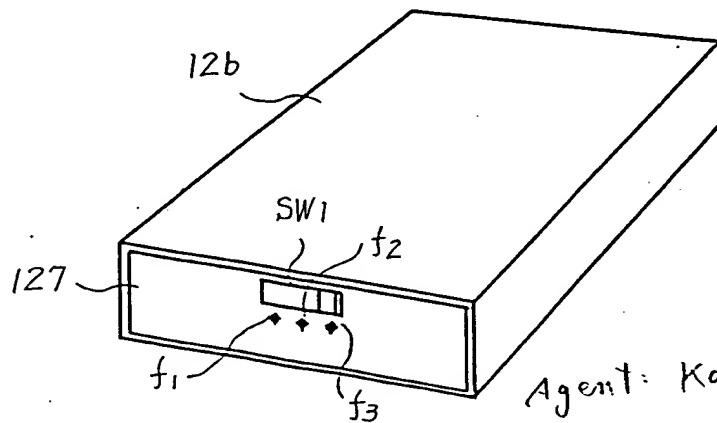
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第 14 図 Fig. 14



第 15 図 Fig. 15

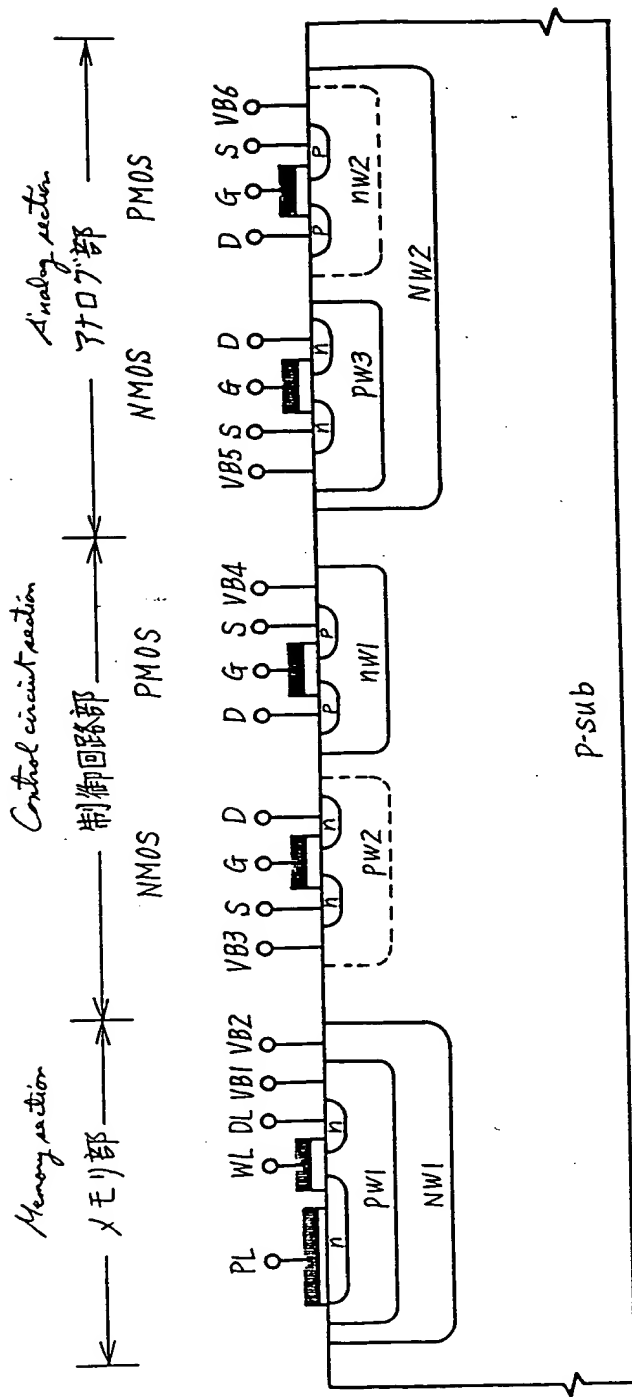


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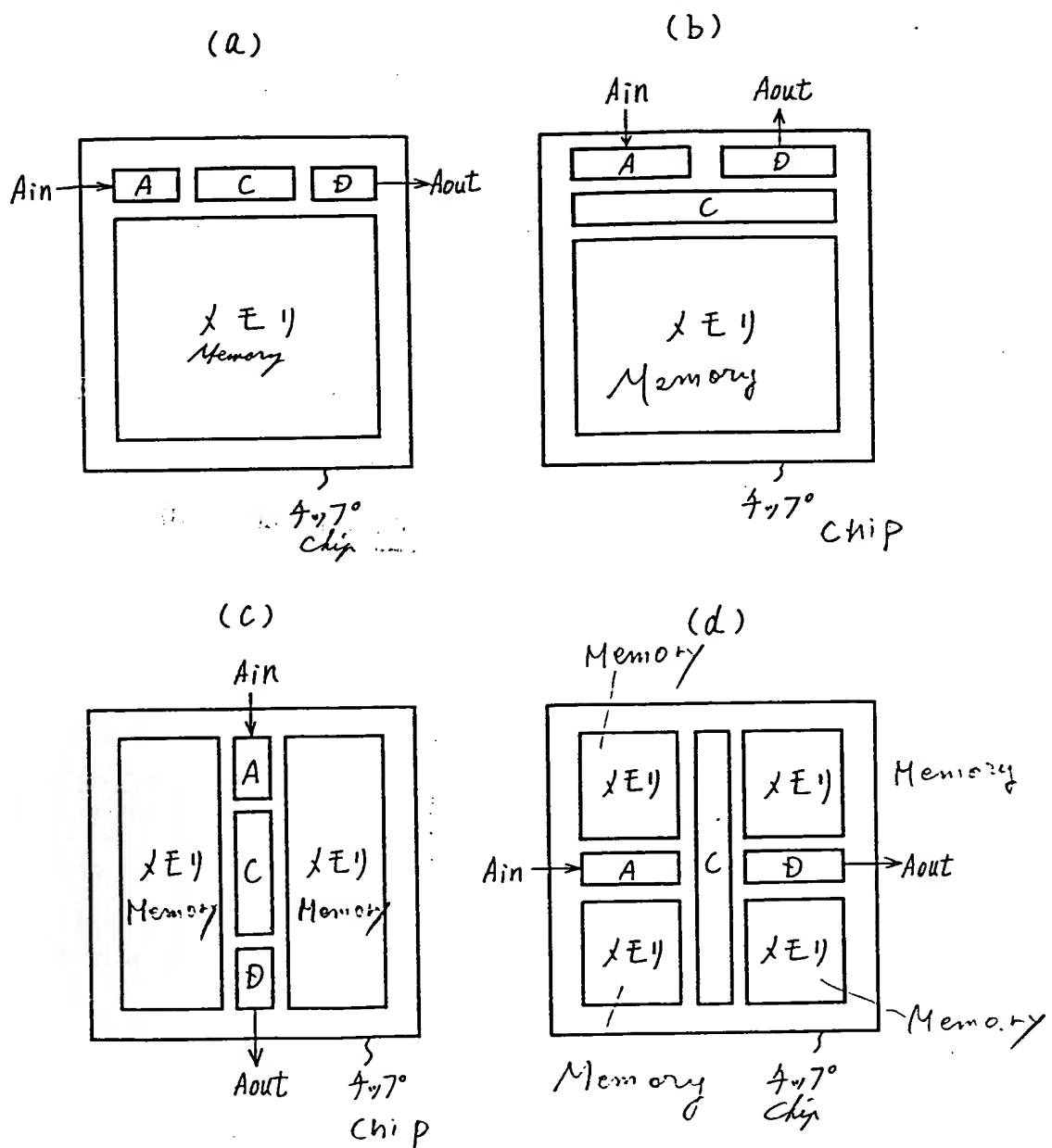


Fig. 6 第 16 区



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第 17 図 Fig. 17



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